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D-LINK SYSTEMS, INC. (Case No. Cv-05-00098-VRW)

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

3COM CORPORATION, Plaintiff/Counterdefendant, v. D-LINK SYSTEMS INC., and REALTEK SEMICONDUCTOR CORPORATION Defendants/Counterplaintiffs.	Case No. Cv-03-2177-VRW **AMENDED FINAL JOINT CLAIM CONSTRUCTION AND PRE-HEARING STATEMENT**

3COM CORPORATION, Plaintiff/Counterdefendant, v. D-LINK SYSTEMS INC., Defendant/Counterplaintiff.	Case No. Cv-05-00098-VRW **AMENDED FINAL JOINT CLAIM CONSTRUCTION AND PRE-HEARING STATEMENT**

Plaintiff/Counterdefendant 3Com Corporation and Defendants/Counterplaintiffs Realtek Semiconductor Corporation and D-Link Systems Inc., by and through respective counsel, hereby respectfully submit the following Amended Final Joint Claim Construction and Pre-Hearing Statement pursuant the Court's Standing Order 3.1.

Table of Contents

I. PATENT L.R. 4-3(b): DISPUTED CLAIM TERMS, PHRASES AND CLAUSES

Pursuant to Patent L.R. 4-3(b), the parties identify the following claim terms, phrases, or clauses on which they disagree, and submit these terms for construction by the Court:

A. Claim Terms not Asserted by Parties as Subject to Construction According to 35 U.S.C. § 112 ¶ 6

1. U.S. Pat. No. 5,307,459

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**alterable storage location**" found in claim numbers: '459 patent: 1	PROPOSED CONSTRUCTION: storage location whose value is changeable DICTIONARY/TREATISE DEFINITIONS: alter: The American Heritage Dictionary of the English Language (4th ed. 2000): v. tr. To change or make different; modify: altered my will. intr. To change or become different. INTRINSIC EVIDENCE: Claims: see, e.g., claim 5 (depending from claim 1, claim 5 claiming posting status information which may be used by the host processor as feedback); claim 1; claim 7, claim 22; claim 23; claim 34; claim 35; claim 40; claim 41; claim 44; claim 45; claim 50; claim 51; claim 52; claim 53; Specification: see, e.g., fig. 2, 14-24; col. 2:47-50 ("The threshold logic includes a counter coupled to the buffer memory for counting the data transfer to or from the buffer memory, and an alterable storage location containing a threshold value."); 3:8-14 ("According to another aspect of the present invention, the network interface logic includes control means for generating an interrupt signal to the host processor responsive to the indication signal. The control means also posts status information which may be used by the host processor as feedback for optimizing the threshold value in the alterable storage location."); see also col. 2:50-54; col. 3:18-25; col. 3:37-56; col. 3:67-4:2; col. 4:7-11; col. 6:32-33; col. 6:38-59; col. 23:56-59; col. 29:64-67; col. 30:45-48; col. 31:7-24; col. 42:19-22; Col. 1: 46-51; Col. 1: 63-66; Col. 2: 46-54; Col. 2: 30-35; Col. 2: 23-27; Col. 6: 9-59; Col. 41:44-55; Col. 3:11-14; Col. 42:17-25; Col. 6: 9-59; Col. 42:17-25; see also Prosecution History: Notice of	PROPOSED CONSTRUCTION: storage location whose value is dynamically changeable INTRINSIC EVIDENCE: '459 patent at 42:17-25 ("*The above indication signals are further optimized by allowing the host processor to dynamically tune the timing of the indication signals. The host processor* has write access to the threshold registers and *may alter the threshold values in the threshold registers based on posted status information by the network adapter*. The posted status information will *allow the host processor to determine whether it is responding too early or too late to an interrupt generated by the indications*.") '459 patent at 6:31-59 ("*Threshold logic 10 contains an alterable storage location 10a which contains a threshold value.* This threshold value represents the amount of a data frame which will be transferred into or out of buffer 9 before an early indication signal will be generated which may cause host interface logic 8 to send an interrupt to host processor 5. . . . *The threshold logic also includes a means for the host processor 5 to dynamically alter the time at which an indication is generated based on prior host processor 5 responses*. When responding to an interrupt generated by an early indication, the host processor may examine network adapter status information to determine if host processor 5 is servicing the interrupt too early or too late. If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame.") '459 patent at 3: 11-14 ("The control means also posts status information which may be used by the host processor as feedback for optimizing the threshold value in the alterable storage location.") '459 patent at 41: 44-55 ("Therefore, the present invention reduces host processor interrupt latency by generating early indications of data frame transfers. These early indications then may be used to generate an early interrupt to the host processor before the data frame is transferred which allows the host processor to save its current environment during a data frame transfer. . . .") '459 patent at 31:7-24: ("3. Determine the latency delta. If the current interrupt and the previous interrupt occurred on the same side of the event (both early or both late), then the latency delta is doubled (multiplied by 2). If the current interrupt occurred on the opposite side of the event (early versus late), then the delta is reset to 1 and has its sign changed. For example, if the current delta is plus 64, then the new delta will be minus 1; if the current delta is negative 32, then the new delta will be plus 1. This assures that if the algorithm overshoots the mark, it will stop and begin to accelerate in the opposite direction. 4. Update threshold value. Finally, *the latency delta is added to the contents of the alterable storage location containing the threshold value*. The algorithm then returns to step 2. The above algorithm may be used for tuning of other threshold logic embodiments which follow.")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		'459 patent at 42:17-25: ("The above indication signals are further optimized by allowing the host processor to dynamically tune the timing of the indication signals. The host processor *has write access to the threshold registers and may alter the threshold values in the threshold registers based on posted status information* by the network adapter. The posted status information will allow the host processor to determine whether it is responding too early or too late to an interrupt generated by the indications.") *See also* Prosecution History: Notice of Allowability, Oct. 14, 1993 DICTIONARY/TREATISE DEFINITIONS: Webster's Ninth New Collegiate Dictionary (Ninth Edition, 1988) Alter: 1: to make different without changing into something else 2: CASTRATE SPAY ~ vi: to become different syn see CHANGE; alterable – adj. Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.
"**buffer**" or "**buffer memory**" found in claim numbers: '459 patent: 1 also presented for construction in: '872 patent: 1, 10, 21 '094 patent: 1, 9, 21, 28, 39, 47	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: buffer: The American Heritage Dictionary of the English Language (4th ed. 2000): A device or area used to store data temporarily; see also Dictionary of Computing (3d ed. 1990): A temporary memory for data, normally used to accommodate the difference in the rate at which two devices can handle data during a transfer; Dictionary of Computing (1st ed. 1983): A temporary memory for data, normally used to accommodate the difference in the rate at which two devices can handle data during a transfer. The buffer may be built into a peripheral device, such as a printer or disk drive, or may be part of the system's main memory; IBM Dictionary of Computing (10th ed. 1993): 1. A routine or storage used to compensate for a difference in rate of flow of data, or time of occurrence of events, when transferring data from	PROPOSED CONSTRUCTION: A memory that (1) stores frame data such that the frame data can be retrieved independently of the order in which the frame data were stored and the frame data can always be retained and reused; and (2) is not a first-in-first-out (FIFO) system. INTRINSIC EVIDENCE: '872 patent at 1:47-54; '094 patent at 1:44-50 ("*Transmit data buffers are to be distinguished from first-in-first-out FIFO systems*, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. *The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.*") '872 patent at 1:65-2:2; '094 patent at 1:60-65 ("Furthermore, the prior art systems which use transmit data buffers require the host or sending system to manage the transmit data

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	one device to another. 4. A portion of storage used to hold input or output data temporarily; Microsoft Computer Dictionary (5th ed. 2002): A region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations or devices; Webster's New World Computer Dictionary (10th ed. 2003): A unit of memory given the task of holding information temporarily, especially while waiting for slower components to catch up; memory: The American Heritage Dictionary of the English Language (4th ed. 2000): Computer Science. a. A unit of a computer that preserves data for retrieval. b. Capacity for storing information: two gigabytes of memory; Dictionary of Computing (1st ed. 1983): A device or medium that can retain information for subsequent retrieval. The term is synonymous with storage and store, although it is most frequently used for referring to the internal storage of a computer that can be directly addressed by operating instructions. INTRINSIC EVIDENCE: Claims: see, e.g., claim 6; ("the buffer memory comprises a buffer independent of the host address space"); see also claim 1; claim 2; claim 3; claim 4; claim 11; claim 14; claim 16; claim 18; claim 20; claim 22; claim 24; claim 25; claim 30; claim 32; claim 34; claim 38; claim 39; claim 40; claim 42; claim 43; claim 44; claim 46; claim 47; claim 48; claim 49; claim 50; claim 52; Specification: see, e.g., figs. 2, 6, 7, 9, 11-13 col. 2:38-41 ("The apparatus includes network interface logic for transferring the data frame between the network transceiver and a buffer memory for storing the data frame."); see also col. 1:25-36; col. 1:39-45; col. 2:1-5; col. 2:41-43; col. 2:46-50; col. 2:55-3:7; col. 3:18-22; col. 3:44-46; col. 3:57-67; col. 4:38-48; col. 6:27-32; col. 6:34-38; col. 7:1-2; col. 7:16-20; col. 7:61-63; col. 10:18-25; col. 10:30-32; col. 10:37-40; col. 10:42-45; col. 10:48-51; col. 10:58-61; col. 10:66-68; col. 11:23-26; col. 11:29-36; col. 11:43-47; col. 11:49-52; col. 12:34-37; col. 12:47-49; col. 13:18-21; col. 13:34-41; col. 13:43-49; col.	buffer. A network interface controller transfers data from the host managed transmit data buffer using DMA techniques through a FIFO buffer in the interface controller and on to the network.") '872 patent at 2:7-10; '094 patent at 2:3-5 ("*It is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler FIFO based systems.*") '872 patent at 2:35-55; '094 patent at 2:28-52 ("According to another aspect of the present invention, the transmit buffer includes a transmit descriptor ring, and a transmit data buffer. . . .") '872 patent at 13:17-48; '094 patent at 12:44-13:5 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. . . .") '872 patent, at 1:5-14 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, application Ser. No. 07/921,519, filed 28 Jul. 1992, now U.S. Pat. No. 5,299,313, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 1:5-13 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	13:53-56; col. 13:58-68; col. 14:1-4; col. 14:6-21; col. 14:26-29; col. 14:34-40; col. 14:59-62; col. 15:67-16:8; col. 16:15-20; col. 16:34-37; col. 16:43-55; col. 16:61-62; col. 17:5-9; col. 17:41-47; col. 17:52-53; col. 17:55-59; col. 17:61-62; col. 18:4-7; col. 18:23-27; col. 18:30-34; col. 18:47-51; col. 18:62-66; col. 19:2-17; col. 19:19-26; col. 19:28-32; col. 19:49-51; col. 19:60-68; col. 20:16-22; col. 20:45-48; col. 20:55-58; col. 20:60-68; col. 21:1-3; col. 22:12-14; col. 23:60-64; col. 24:12-15; col. 24:28-30; col. 24:38-44; col. 24:56-59; col. 24:63-68; col. 25:12-19; col. 25:21-24; col. 25:35-41; col. 25:62-63; col. 26:1-3; col. 26:40-42; col. 26:65-67; col. 27:53-55; col. 28:4-6; col. 28:20-22; col. 33:26-33; col. 34:25-28; col. 38:14-17; see also Prosecution History: Notice of Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: See section I.A, supra (agreed upon definition for "buffer" in '884 patent). See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, Ser. No. 07/921,519, filed Jul. 28, 1992, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 13:58-14:22 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission. . . . ") DICTIONARY/TREATISE DEFINITIONS: The Network Interface Technical Guide, (First Edition, 1992) Buffer: A temporary storage area in random access memory where the NIC or computer stores information (usually while transmitting or receiving network traffic). Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules. PRIOR ART: Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor," November 1989, Intel Corp, pg. 2 ("Two large, independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate long bus latencies and provide programmable

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		thresholds that allow the user to optimize bus overhead for any worst-case bus latency.") Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc., pg. 2-37 ("The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory.") 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-295: ("The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network.") Ethernet/IEEE-802.3 Family 1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations The FIFO provides temporary buffer storage for data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the FIFO is 48 bytes. Transmit Data is loaded into the FIFO under internal micro-program control. The FIFO must be more than 16 bytes empty before the ILACC requests the bus (HOLD/BURREQ is asserted). The ILACC will start sending the preamble (if the line is idle) as soon as there is one byte loaded into the FIFO. Should the transmitter be required to back off, there will be up to 32 bytes of data in the FIFO ready for transmission. Reception has priority over transmission during the time that the transmitter is backing off. Receive Data is loaded into the FIFO from the serial input shift register during reception and leaves

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		the FIFO under microprogram control. The ILACC microcode will wait until there are at least 16 bytes of data in the FIFO before initiating a DMA burst transfer. Preamble (including the synchronization bits) is not loaded into the FIFO.")
"**indication signal**" found in claim numbers: '459 patent: 1	PROPOSED CONSTRUCTION: A signal that indicates a subsequent action, such as an interrupt DICTIONARY/TREATISE DEFINITIONS: indication: The American Heritage Dictionary of the English Language (4th ed. 2000): Something that serves to indicate; a sign; signal: The American Heritage Dictionary of the English Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition. INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 21; claim 22; claim 23; claim 31; claim 34; claim 35; claim 40; claim 41; claim 44; claim 45; claim 50; claim 51; claim 52; claim 53; Specification: see, e.g., col. 2:35-38 ("The apparatus is coupled between a network transceiver and a host system which includes a host processor and host memory.");col. 2:52-54 ("The indication signal to the host is generated based on the comparison of the counter and the threshold value in the alterable storage location"); col. 3:7-11 ("According to	PROPOSED CONSTRUCTION: A signal that is not an interrupt but may be used by the host system to generate an interrupt. INTRINSIC EVIDENCE: '459 patent, Abstract ("*Optimized indication signals of a completed data frame transfer are generated by a network adapter which reduces host processor interrupt latency.* . . . The network adapter further includes threshold logic where a threshold value in an alterable storage location is compared to a data transfer counter in order to generate an early indication signal. *The early indication signal may be used to generate an early interrupt signal to a host processor* before a transfer of a data frame is completed. . . . ") '459 patent at 1:20-2:27("2. Description of Related Art Network adapters involved in the transfer of data frames between a communications network and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to view the data frame resident in the network adapter buffer memory before allowing transfer of the data frame to host memory or other host devices on the computer system bus. Moreover, if a determination is made that the data frame will be transferred to the host computer system, *the host processor may require notification of the completion of the transfer of the data frame* from the network adapter buffer memory to the host computer system. Likewise, with respect to the transmission path, the host processor may require notification on the completion of a data frame transfer. The host processor may require notification of the completion of a download of a data frame from a host system to the

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	another aspect of the present invention, the network interface logic includes control means for generating an interrupt signal to the host processor responsive to the indication signal."); col. 3:33-4:12 ("According to yet another aspect of the present invention, the network adapter includes look-ahead threshold logic for generating an early receive indication signal during the receiving of the data frame. The data frame includes a header field followed by a data field. The look-ahead threshold logic includes an alterable storage location containing a look-ahead threshold value representing an amount of data relative to the beginning of the header field. A comparison between the look-ahead threshold value in the alterable storage location and the counter generates an early receive indication signal. View logic is also provided to present the data frame in the buffer memory to the host system prior to transferring to the host memory. Yet, according to another aspect of the present invention, the network adapter includes length-left threshold logic for generating a receive complete indication signal during the receiving of the data frame which includes a header field followed by a data field. The length-left threshold includes an alterable storage location containing a length-left threshold value representing an amount of data relative to the end of the data field. A comparison of the length-left threshold value in the alterable storage location and the counter generates an early receive indication signal. Also, error detection means is provided for checking the data field transferred from the network transceiver to the buffer memory which generates a receive frame status signal. According to another aspect of the present invention, the network adapter includes transfer threshold logic for generating a transfer complete indication signal during the transferring of the data frame from the network buffer memory to the host system. The network buffer memory being independent from the host address space. The transfer threshold logic includes an alterable storage location containing a transfer threshold value	network adapter buffer memory. In addition, a notification to the host processor on the completion of the transmission of a data frame from the network adapter buffer memory onto the communications network may be required. *In prior art systems*, such as the National Semiconductor DP83932B, a systems-oriented network interface controller (SONIC) and the Intel 82586 local area network co-processor, *an interrupt is generated by the network adapter to the host processor on the completion of a data transfer.* The host processor then must determine the cause of the interrupt by examining the appropriate network adapter status registers and take the appropriate action. However, before the host processor services the interrupt, the host processor must save its current environment or system parameters. This routine of saving the host processor's current environment may take as long as 30 .µs for a OS/2 operating system. The period of time necessary for saving the host processor's environment depends upon the type of host processor used, the host computer system configuration and when the interrupt /occurred. *As can be seen, there is interrupt latency between when the network adapter has completed a transfer and when the host processor is able to service the interrupt generated by the network adapter.* In essence, the host system/network adapter performance is in an idle state even though a transfer has been completed because the host processor is saving its current environment. For example, a data frame may have been received and is resident in the network adapter buffer memory for as long as 30 µs before the host processor is able to determine the cause of the interrupt and view the data frame. The host system/network adapter performance degradation introduced by interrupt latency is compounded when multiple data frames are transferred. Between each data frame transfer, there will be an embedded delay period when the network adapter is waiting for the host processor to save its current environment and respond to a network adapter interrupt signal. Performance degradation is further complicated by the dynamic nature of interrupt latency. While interrupt latency is

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	representing an amount of the data frame to be transferred before generating a transfer complete indication."); see also col. 1:20-2:27; col. 41:44-50; col. 42:17-25; col. 2:29-41; col. 6:9-59; col. 5:68-6:22; col. 2:22-26; col. 2:30-39; col. 2:43-50; col. 3:8-11; col. 3:15-18; col. 3:22-36; col. 3:41-43; col. 3:47-51; col. 3:54-57; col. 3:61-65; col. 4:3-7; col. 6:10-15; col. 6:34-40; col. 6:48-60; col. 29:31-39; col. 29:64-66; col. 30:10-13; col. 34:26-40; col. 42:17-19; see also Prosecution History: Notice of Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	relatively constant given a periodic interrupt, interrupt latency may increase substantially in the form of spikes depending upon when the interrupt occurred. Moreover, the host computer system configuration may be altered by installation of additional software or devices on the system bus which will increase interrupt latency. *Therefore, it is desirable to provide a network adapter with an optimized indication signal to the host processor of the completion of the transfer of a data frame which reduces interrupt latency allowing for optimized network adapter/host system performance.*") '459 patent at 2:29-41 ("The present invention provides for optimized indication signals to a host processor by a network adapter of the completion of a transfer of a data frame. The apparatus is coupled between a network transceiver and a host system which includes a host processor and host memory. The apparatus generates an indication signal to the host processor responsive to the transfer of a data frame. The host processor responds to the indication signal after a period of time. The apparatus includes network interface logic for transferring the data frame between the network transceiver and a buffer memory for storing the data frame.") '459 patent at 6:9-59 ("Threshold logic 10 in network adapter 3 is designed for eliminating or reducing interrupt latency. Threshold logic 10 makes a determination of how much of a data frame is transferred before generating an early indication signal. *The early indication signal may then cause an early interrupt signal to be generated during the transfer of a data frame.* Moreover, threshold logic 10 is designed such that the time required for transferring the remainder of the data frame should approximately equal the time required for host processor 5 save its system parameters. Therefore, interrupt latency is eliminated or reduced by allowing host processor 5's interrupt routine to coincide with the transfer of the remainder of the data frame. FIG. 2 is a functional block diagram of network adapter 3 with threshold logic 10 illustrating the various transfer paths. Network adapter 3 contains transceiver 12 which transmits and receives data frames across

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		network 2. Network interface logic 11 is responsible for the transfer of a data frame between network buffer 9 and transceiver 12. Likewise, the network adapter 3 contains host interface logic 8 which is responsible for transferring a data frame between network buffer 9 and host system 1. Threshold logic 10 contains an alterable storage location 10a which contains a threshold value. This threshold value represents the amount of a data frame which will be transferred into or out of buffer 9 before an early indication signal will be generated which may cause host interface logic 8 to send an interrupt to host processor 5. Host processor 5 has access to the alterable storage 10a location containing the threshold value through host interface logic 8. The threshold logic also includes a means for the host processor 5 to dynamically alter the time at which an indication is generated based on prior host processor 5 responses. When responding to an interrupt generated by an early indication, the host processor may examine network adapter status information to determine if host processor 5 is servicing the interrupt too early or too late. If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame.") '459 patent at 5:68-6:22 ("Typically, devices on host bus 4, such as network adapter 3, request service from host processor 5 by generating an interrupt on host bus 4. The host processor 5 then must save its system parameters and determine which device caused the interrupt and what service is required. Interrupt latency is introduced from when a device such as network adapter 3 generates an interrupt signal and when host processor 5 is able to service the device.

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		Threshold logic 10 in network adapter 3 is designed for eliminating or reducing interrupt latency. Threshold logic 10 makes a determination of how much of a data frame is transferred before generating an early indication signal. The early indication signal may then cause an early interrupt signal to be generated during the transfer of a data frame. Moreover, threshold logic 10 is designed such that the time required for transferring the remainder of the data frame should approximately equal the time required for host processor 5 save its system parameters. Therefore, interrupt latency is eliminated or reduced by allowing host processor 5's interrupt routine to coincide with the transfer of the remainder of the data frame.") '459 patent; at 41:44-50 ("Therefore, the present invention reduces host processor interrupt latency by generating early indications of data frame transfers. These early indications then may be used to generate an early interrupt to the host processor before the data frame is transferred which allows the host processor to save its current environment during a data frame transfer.") <u>DICTIONARY/TREATISE DEFINITIONS:</u> <u>signal</u> <u>Newton's' Telecom Dictionary (fourth edition, 1991)</u> Signal: 1. An electrical wave used to convey information 2. An alert. 3. An acoustic device (e.g. a bell) or a visual device (e.g. a lamp) which calls attention. To transmit an information signal or alerting signal. <u>McGraw Hill Electronics Dictionary (fifth edition, 1994)</u> Signal: Any variation in an electrical current, visible or nonvisible light, audible or ultrasonic energy that conveys information. Signals can be coded in frequency, phase, or amplitude to separate them from unwanted noise. Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.

2. U.S. Pat. No. 5,434,872

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**falls behind**" or "**underrun**" found in claim numbers: '872 patent: 1 also presented for construction in: '094 patent: 21	PROPOSED CONSTRUCTION: When expected data from a frame to be transferred is not available in a buffer DICTIONARY/TREATISE DEFINITIONS: IBM Dictionary of Computing (10th ed. 1993): Loss of data caused by inability of a transmitting device or channel to provide data to the communication control logic (SDLC or BSC/SS) at a rate that is fast enough for the attached data link or loop; see also The American Heritage Dictionary of the English Language (4th ed. 2000): Something that runs under, as: a. An amount or a quantity produced that is less than what has been estimated. b. The difference between this amount or quantity and what has been estimated. INTRINSIC EVIDENCE: Claims: see, e.g., claim 15 ("an underrun condition in which the host interface means in transferring data to the buffer memory falls behind the network interface means in transferring data to the transceiver"); claim 25 ("a condition in which the data transfer circuitry falls behind the medium access controller"); see also claim 1; claim 18; claim 24; Specification: fig. 18; col. 28:48-29:2 ("According to the present invention, this transmit data path includes an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer, by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. The underrun detector 413 is controlled by the transmit control logic 411. The transmit control logic 411 indicates intervals across line 414 on line 402. The underrun detector determines that a transmit write TXWR signal in not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. In response to the bad frame signal, the CRC data is inverted by the exclusive OR gate 407 which causes a bad CRC to be generated for the already transmitted portions of the frame suffering the underrun. Transmit control logic 411 also responds to the bad frame signal on line 409 to select the bad CRC data through multiplexer 410.	PROPOSED CONSTRUCTION: A condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2 ("According to the present invention, this transmit data path includes *an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer*, . . . , *by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic*. . . . The underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. . . . ") '872 patent at claim 1 ("… underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition.) '872 patent at claim 15 ("…underrun control logic, which detects an underrun condition in which the host interface means in transferring data to the buffer memory falls behind the network interface means in transferring data to the transceiver, and means for supplying a bad frame signal to the communication media in response to the underrun condition.") '872 patent at claim 18 (…underrun control means, coupled with the network interface means, for detecting an underrun condition in which the host interface means in downloading data to the transmit data buffer falls behind the network interface means in transferring data to the transceiver, and for supplying a bad frame signal to the network transceiver in response to the underrun condition.")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Finally, the bad frame signal on line 409 in used for posting status information through the xmitFailureRegister of an underrun condition."); col. 9:40-43; col. 19:35-38; col. 28:58-60; see also Prosecution History: Office Action, Oct. 26, 1993, p. 3; Response to Office Action, Oct. 5, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,307,459; 5,732,094; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	'872 patent at claim 24 ("…underrun control logic, which detects a condition in which the data transfer circuitry falls behind the medium access controller, and supplies a bad frame signal to the network in response to the underrun condition.") '094 patent at claim 4 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the network; and supplying a bad frame signal to the network un response to the underrun condition.") '094 patent at claim 16 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the communications medium; and supplying a bad frame signal to the communications medium in response to the underrun condition.") '094 patent at claim 34 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the network transceiver; and supplying a bad frame signal to the network transceiver in response to the underrun condition.") '094 patent at claim 41 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the network; and supplying a bad frame signal to the network in response to the underrun condition.") Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.
"**buffer**" or "**buffer memory**" found in claim numbers:	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer**" and "**memory**" in subsection 1.	PROPOSED CONSTRUCTION: A memory that (1) stores frame data such that the frame data can be retrieved independently of the order in which the frame data were stored and the frame data can always be retained and reused and can be accessed by the host

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
'872 patent: 1, 10, 21 also presented for construction in: '459 patent: 1 '094 patent: 1, 9, 21, 28, 39, 47	INTRINSIC EVIDENCE: Claims: see, e.g., claim 2 ("the transmit buffer includes a transmit descriptor ring and a *transmit data buffer*"); claim 7 ("The apparatus of claim 1, wherein the buffer includes a transmit descriptor ring buffer and a transmit data buffer, and the means for transferring includes: transmit descriptor logic for mapping transmit descriptors from the system to the transmit descriptor ring buffer; and download logic, responsive to the transmit descriptors in the transmit descriptor ring buffer, for retrieving data from memory in the system and storing retrieved data in the transmit data buffer."); see also claim 1; claim 3; claim 9; claim 10; claim 11; claim 15; claim 18; claim 21; claim 22; Specification: see, e.g., figs. 2, 6-10E; col 1:47-54 ("Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers."); col. 1:65-67 ("Furthermore, the prior art systems which use transmit data buffers require the host or sending system to manage the transmit data buffer."); col. 2:13-18 ("The present invention provides for the early initiation of transmission of data in a network interface that includes a dedicated transmit buffer."); col. 2:35-37 ("the transmit data buffer includes a transmit descriptor ring, and a transmit data buffer"); col. 13:12-27 ("In the preferred system, the adapter uses 32K bytes of static RAM for the transmit buffers, receive buffers, control structures, and various status and statistics registers. Several of the regions in the adapter's memory defined in Fig. 5 provide defined data structures. A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffer closest to the base of the memory as the power up	system; and (2) is not a first-in-first-out (FIFO) system. INTRINSIC EVIDENCE: '872 patent at 1:47-54; '094 patent at 1:44-50 ("*Transmit data buffers are to be distinguished from first-in-first-out FIFO systems*, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. *The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.*") '872 patent at 1:65-2:2; '094 patent at 1:60-65 ("Furthermore, the prior art systems which use transmit data buffers require the host or sending system to manage the transmit data buffer. A network interface controller transfers data from the host managed transmit data buffer using DMA techniques through a FIFO buffer in the interface controller and on to the network.") '872 patent at 2:7-10; '094 patent at 2:3-5 ("*It is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler FIFO based systems.*") '872 patent at 2:35-55; '094 patent at 2:28-52 ("According to another aspect of the present invention, the transmit buffer includes a transmit descriptor ring, and a transmit data buffer. . . .") '872 patent at 13:17-48; '094 patent at 12:44-13:5 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . .

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	default."); see also col. 1:36-2:10; col. 2:14-27; col. 2:44-48; col. 3:21-27; col. 3:59-65; col. 4:29-33; col. 4:38-45; col. 4:64-5:22; col. 5:41-43; col. 5:57-61; col. 6:33-35; col. 8:57-64; col. 9:1-3; col. 9:8-11; col. 9:13-16; col. 9:19-22; col. 9:29-32; col. 9:37-39; col. 9:62-65; col. 9:68-10:7; col. 10:16-18; col. 10:20-23; col. 11:17-20; col. 11:22-25; col. 11:33-39; col. 11:59-61; col. 12:4-6; col. 12:43-46; col. 12:58-68; col. 13:2-8; col. 13:12-15; col. 13:17-48; col. 13:52-54; col. 13:61-66; col. 14:17-20; col. 15:25-46; col. 15:58-60; col. 16:1-7; col. 16:9-12; col. 16:28-32; col. 16:35-39; col. 16:52-56; col. 16:67-17:3; col. 17:7-22; col. 17:24-31; col. 17:33-34; col. 17:54-56; col. 17:65-68; col. 18:21-25; col. 18:44-46; col. 18:49-52; col. 19:45-47; col. 21:22-26; col. 21:42-45; col. 22:60-62; col. 22:1-2; col. 22:4-8; col. 22:20-23; col. 22:27-32; col. 22:44-51; col. 22:53-56; col. 22:67-23:4; col. 23:43-45; col. 23:48-51; col. 23:60-65; col. 24:26-27; col. 24:29-32; col. 24:37-39; col. 24:39-40; col. 24:43-52; col. 25:48-50; col. 28:48-54; col. 29:5-9; col. 29:25-31; see also Prosecution History: Office Action, Oct. 26, 1993, p. 2; Office Action, Oct. 26, 1993, p. 3; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Office Action, Oct. 26, 1993, p. 6; Part 131 Affidavit, p. 1; Part 131 Affidavit, p. 2; Part 131 Affidavit, p. 3; Part 131 Affidavit, p. Ex. 1, p. 6; Response to Office Action, Feb. 23, 1994, p. 2; Response to Office Action, Feb. 23, 1994, pp. 4-5; Response to Office Action, Feb. 23, 1994, p. 5; Response to Office Action, Feb. 23, 1994, p. 6; Office Action, Jul. 6, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 3. EXTRINSIC EVIDENCE: See also section I.A, supra (agreed upon definition for "buffer" in '884 patent); U.S. Patent Nos. 5,307,459; 5,732,094; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement	The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. . . .") '872 patent, at 1:5-14 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, application Ser. No. 07/921,519, filed 28 Jul. 1992, now U.S. Pat. No. 5,299,313, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 1:5-13 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, Ser. No. 07/921,519, filed Jul. 28, 1992, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 13:58-14:22 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a

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	made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission. . . . ") DICTIONARY/TREATISE DEFINITIONS: The Network Interface Technical Guide, (First Edition, 1992) Buffer: A temporary storage area in random access memory where the NIC or computer stores information (usually while transmitting or receiving network traffic). PRIOR ART: Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor," November 1989, Intel Corp, pg. 2 ("Two large, independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency.") Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc., pg. 2-37 ("The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory.") 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-295: ("The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network.")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		Ethernet/IEEE-802.3 Family 1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations The FIFO provides temporary buffer storage for data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the FIFO is 48 bytes. Transmit Data is loaded into the FIFO under internal micro-program control. The FIFO must be more than 16 bytes empty before the ILACC requests the bus (HOLD/BURREQ is asserted). The ILACC will start sending the preamble (if the line is idle) as soon as there is one byte loaded into the FIFO. Should the transmitter be required to back off, there will be up to 32 bytes of data in the FIFO ready for transmission. Reception has priority over transmission during the time that the transmitter is backing off. Receive Data is loaded into the FIFO from the serial input shift register during reception and leaves the FIFO under microprogram control. The ILACC microcode will wait until there are at least 16 bytes of data in the FIFO before initiating a DMA burst transfer. Preamble (including the synchronization bits) is not loaded into the FIFO.") Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.
"**optimizing the threshold**" found in claim numbers: '872 patent: 10 also presented for construction in: '094 patent: 21	PROPOSED CONSTRUCTION: Attempting to make the transmission of frames more efficient. DICTIONARY/TREATISE DEFINITIONS: threshold: The American Heritage Dictionary of the English Language (4th ed. 2000): The point that must be exceeded to begin producing a given effect or result or to elicit a response; see also Dictionary of Computing (1st ed. 1983): Threshold element: A logic element whose output is determined by comparing a weighted sum of inputs with a predetermined/prescribed	PROPOSED CONSTRUCTION: Dynamically changing the threshold value by the host system to make it as perfect, effective, or functional as possible. INTRINSIC EVIDENCE: '872 patent, Abstract; '094 patent, Abstract ("The monitoring logic includes *a threshold store, which is programmable by the host computer* for storing a threshold value. Thus, *the threshold value may be set by the host system to optimize performance in a given setting.*")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	threshold value. If the threshold is exceeded, the output is a logic 1; if not, the output is logic 0. If the number of inputs is odd, if the weights are all equal, and the threshold is equal to half of the number of inputs, then the threshold element behaves as a majority element. A system of threshold elements is described by or as threshold logic; optimize: The American Heritage Dictionary of the English Language (4th ed. 2000): Optimize: Computer Science. To increase the computing speed and efficiency of (a program), as by rewriting instructions; see also Microsoft Computer Dictionary (5th ed. 2002): Optimization: 1. In programming, the process of producing more efficient (smaller or faster) programs through selection and design of data structures. 2. The process of a compiler or assembler in producing efficient executable code. INTRINSIC EVIDENCE: Claims: claim 10; claim 19; Specification: figs. 2, 4, 13, 14, 17, 18; col. 29:35-38 ("If this register set to zero, then the early transmit feature is disabled and the entire transmit frame must reside on the adapter before the adapter will begin to transmit it"); col. 29:48-51 ("If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register"); see also col. 29:12-57; col. 4:46-55; col. 2:27-34; col. 2:31-34; col. 4:58-60; col. 29:39-40; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Part 131 Affidavit, p. Ex. 1, p. 6; Response to Office Action, Feb. 23, 1994, p. 2. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459; 5,732,094; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules.	'872 patent at 2:27-34; '094 patent at 2: 21-27 ("In one aspect of the invention, the monitoring logic includes *a threshold store, which is programmable by the host computer for storing a threshold value* and logic for posting status information to the host. Thus, *the threshold value may be set by the host system to optimize performance using the alterable threshold store* and the posted status information.") '872 patent at 4:46-55; '094 patent at 4:38-46 ("*The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30.* In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31. *Alternatively, the threshold store may be a read only memory set during manufacture.* In yet other alternatives, the threshold store *may be implemented using user specified data* in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices.") '872 patent at 29:12-57; '094 patent at 27:44-28:-17 ("XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, . . ., before the adapter can commence with the media access control functions associated with transmitting the frame. . . . The value for this register *may be programmed by the host to optimize performance*. . . . The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. . . .") DICTIONARY/TREATISE DEFINITIONS: See "**altering the threshold**" for definitions of "threshold." Optimize: Webster's Ninth New Collegiate

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	Dictionary, (ninth edition, 1988) Optimize: to make as perfect, effective, or functional as possible. Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.

3. U.S. Pat. No. 5,732,094

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**buffer**" or "**buffer memory**" found in claim numbers: '094 patent: 1, 9, 21, 28, 39, 47 also presented for construction in: '459 patent: 1 '872 patent: 1, 10, 21	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer**" and "**memory**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 33 ("The method as in claim 28, wherein the initiating transmission of the frame step includes: retrieving data from the buffer memory; and supplying the retrieved data for transmission to the network transceiver."); see also claim 1; claim 4; claim 6; claim 7; claim 9; claim 10; claim 11; claim 14; claim 16; claim 20; claim 21; claim 28; claim 29; claim 30; claim 34; claim 38; claim 39; claim 41; claim 44; claim 45; claim 47; claim 49; claim 52; Specification: see, e.g., figs. 2, 6-10E; col. 1:44-50 ("Transmit data buffers are to be distinguished from first-in-first-out FIFO systems in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission."); col. 2:28-30 ("the transmit data buffer includes a transmit descriptor ring, and a transmit data buffer") and other quotes from **"buffer"** in subsection 2 above, which also appear in the specification of the '094, since it is a continuation of the '872; see also col. 1:29-33; col. 1:35-37; col. 1:38-50; col. 1:51-56; col. 1:56-58; col. 1:60-62; col. 2:3-5; col. 2:7-9; col. 2:11-20; col. 2:35-39; col. 3:14-33; col. 4:55-5:12; col. 5:31-32; col. 5:45-47; col. 6:20-22; col. 8:31-33; col. 8:34-37; col. 8:44-46; col. 8:48-51; col. 8:53-56; col. 8:58-61; col. 8:66-9:3; col. 9:8-10; col. 9:33-35; col. 9:38-43; col. 9:50-54; col. 9:56-59; col. 10:50-53; col. 10:55-58; col. 10:65-67;	PROPOSED CONSTRUCTION: A memory that (1) stores frame data such that the frame data can be retrieved independently of the order in which the frame data were stored and the frame data can always be retained and reused and can be accessed by the host system; and (2) is not a first-in-first-out (FIFO) system. INTRINSIC EVIDENCE: '872 patent at 1:47-54; '094 patent at 1:44-50 ("*Transmit data buffers are to be distinguished from first-in-first-out FIFO systems*, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. *The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.*") '872 patent at 1:65-2:2; '094 patent at 1:60-65 ("Furthermore, the prior art systems which use transmit data buffers require the host or sending system to manage the transmit data buffer. A network interface controller transfers data from the host managed transmit data buffer using DMA techniques through a FIFO buffer in the interface controller and on to the network.") '872 patent at 2:7-10; '094 patent at 2:3-5 ("*It is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler FIFO based systems.*")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	col. 11:1-4; col. 11:23-25; col. 11:34-37; col., 12:4-8; col. 12:18-28; col. 12:30-36; col. 12:39-41; col. 12:44-52; col. 12:54-13:5; col. 13:9-11; col. 13:17-21; col. 13:39-47; col. 14:52-54; col. 14:57-59; col. 15:8-10; col. 15:16-18; col. 15:20-22; col. 15:24-27; col. 15:42-45; col. 15:48-52; col. 15:64-67; col. 16:11-14; col. 16:18-22; col. 16:23-33; col. 16:35-42; col. 16:44-48; col. 16:63-65; col. 17:6-9; col. 17:30-34; col. 17:51-52; col. 17:55-58; col. 18:47-50; col. 20:19-22; col. 20:39-41; col. 20:56-57; col. 20:63-66; col. 20:67-21:3; col. 21:15-18; col. 21:22-27; col. 21:39-45; col. 21:47-50; col. 21:59-64; col. 22:33-35; col. 22:38-41; col. 22:49-53; col. 23:13-18; col. 23:24-27; col. 23:25-28; col. 23:28-31; col. 23:33-37; col. 24:27-30; col. 27:16-19; col. 27:39-42; col. 27:57-61; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 53; Specification as Filed, p. 54; Specification as Filed, p. 55; Specification as Filed, p. 56; Specification as Filed, p. 57; Preliminary Amendment, Mar. 3, 1995, p. 2; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 2; Office Action, Mar. 19, 1996, p. 3; Office Action, Mar. 19, 1996, p. 4; Office Action, Mar. 19, 1996, p. 5; Office Action, Mar. 19, 1996, p. 6; Office Action, Mar. 19, 1996, p. 7; Office Action, Mar. 19, 1996, p. 8; Office Action, Jan. 7, 1997, p. 2; Response to Office Action, Apr. 7, 1997, pp. 1-2; Response to Office Action, Apr. 7, 1997, p. 5. EXTRINSIC EVIDENCE: See section I.A, supra (agreed upon definition for "buffer" in '884 patent); U.S. Patent Nos. 5,307,459, 5,434,872; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to	'872 patent at 2:35-55; '094 patent at 2:28-52 ("According to another aspect of the present invention, the transmit buffer includes a transmit descriptor ring, and a transmit data buffer. . . .") '872 patent at 13:17-48; '094 patent at 12:44-13:5 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. . . .") '872 patent, at 1:5-14 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, application Ser. No. 07/921,519, filed 28 Jul. 1992, now U.S. Pat. No. 5,299,313, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 1:5-13 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, Ser. No. 07/921,519, filed Jul. 28, 1992, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 13:58-14:22

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission. . . . ") <u>DICTIONARY/TREATISE DEFINITIONS</u>: <u>The Network Interface Technical Guide, (First Edition, 1992)</u> Buffer: A temporary storage area in random access memory where the NIC or computer stores information (usually while transmitting or receiving network traffic). <u>PRIOR ART:</u> Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor," November 1989, Intel Corp, pg. 2 ("Two large, independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency.") Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc., pg. 2-37 ("The transmit FIFO (Figure 1) is a 36-bit

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory.") 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-295: ("The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network.") Ethernet/IEEE-802.3 Family 1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations The FIFO provides temporary buffer storage for data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the FIFO is 48 bytes. Transmit Data is loaded into the FIFO under internal micro-program control. The FIFO must be more than 16 bytes empty before the ILACC requests the bus (HOLD/BURREQ is asserted). The ILACC will start sending the preamble (if the line is idle) as soon as there is one byte loaded into the FIFO. Should the transmitter be required to back off, there will be up to 32 bytes of data in the FIFO ready for transmission. Reception has priority over transmission during the time that the transmitter is backing off. Receive Data is loaded into the FIFO from the serial input shift register during reception and leaves the FIFO under microprogram control. The ILACC microcode will wait until there are at least 16 bytes of data in the FIFO before initiating a DMA burst

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		transfer. Preamble (including the synchronization bits) is not loaded into the FIFO.") Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.
"**optimizing the threshold**" found in claim numbers: '094 patent: 21 also presented for construction in: '872 patent: 10	PROPOSED CONSTRUCTION: Attempting to make the transmission of frames more efficient. DICTIONARY/TREATISE DEFINITIONS: See "**optimizing the threshold**" in subsection 2. INTRINSIC EVIDENCE: Claims see claim 8; claim 13; claim 21; claim 31; claim 46; claim 48; Specification: see, e.g., figs. 2, 4, 13, 14, 17, 18; col. 2:24-27 ("the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information"); col. 4:38-41; col. 4:49-51; col. 28:1-2; col. 27:65-67; col. 4:38-46 ; col. 2: 21-27 ; col. 27:44-28:17; see also Prosecution History: Specification as Filed, p. 55; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 4; Response to Office Action, Apr. 7, 1997, p. 2. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459, 5,434,872; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand	PROPOSED CONSTRUCTION: Dynamically changing the threshold value by the host system to make it as perfect, effective, or functional as possible. INTRINSIC EVIDENCE: '872 patent, Abstract; '094 patent, Abstract ("The monitoring logic includes *a threshold store, which is programmable by the host computer* for storing a threshold value. Thus, *the threshold value may be set by the host system to optimize performance in a given setting.*") '872 patent at 2:27-34; '094 patent at 2: 21-27 ("In one aspect of the invention, the monitoring logic includes *a threshold store, which is programmable by the host computer for storing a threshold value* and logic for posting status information to the host. Thus, *the threshold value may be set by the host system to optimize performance using the alterable threshold store* and the posted status information.") '872 patent at 4:46-55; '094 patent at 4:38-46 ("*The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30.* In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31. *Alternatively, the threshold store may be a read only memory set during manufacture.* In yet other alternatives, the threshold store *may be implemented using user specified data* in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices.") '872 patent at 29:12-57; '094 patent at 27:44-28:-17 ("XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, . . ., before the adapter can commence with the media access control functions associated with transmitting the

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	this term. 3Com reserves the right to rely on testimony by any expert in this action..	frame. . . . The value for this register *may be programmed by the host to optimize performance*. . . . The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. . . .") DICTIONARY/TREATISE DEFINITIONS: See "**altering the threshold**" for definitions of "threshold." Optimize: Webster's Ninth New Collegiate Dictionary, (ninth edition, 1988) Optimize: to make as perfect, effective, or functional as possible. Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.
"**underrun**" or "**falls behind**" found in claim numbers: '094 patent: 21 also presented for construction in: '872 patent: 1	PROPOSED CONSTRUCTION: When expected data from a frame to be transferred is not available in a buffer DICTIONARY/TREATISE DEFINITIONS: See "**underrun**" in subsection 2. INTRINSIC EVIDENCE: Claims: see, e.g., claim 8 ("The method as in claim 7, further comprising: providing access to the threshold value so that it may be dynamically programmed by the host system; and posting status information for use by the host system as feedback for optimizing the threshold value."); claim 22 ("The method as in claim 21, wherein the threshold amount is dynamically programmable by the host computer."); claim 30 ("The method as in claim 28, wherein the threshold determination is based on a comparison of the amount of data transferred into the buffer memory with a threshold value, the threshold value being dynamically programmable by the host system."); see also claim 4; claim 6; claim	PROPOSED CONSTRUCTION: A condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2 ("According to the present invention, this transmit data path includes an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer, by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. . . . The underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. . . . ") '872 patent at claim 1 ("… underrun

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	16; claim 20; claim 21; claim 34; claim 38; claim 41; claim 44; claim 52; claim 53; Specification: see, e.g., fig. 18; col. 4:50-52; col. 7:62-4; col. 9:11-14; col. 14:22-23; col. 18:26-42; col. 22:10-12; col. 26:60-61; col. 27:16-21; col. 27:21-23; col. 27:24-32; col. 27:34-36; col. 28:2-5; col. 28:7-17; see also Prosecution History: Specification as Filed, p. 53; Specification as Filed, p. 54; Specification as Filed, p. 56; Specification as Filed, p. 57; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 3; Response to Office Action, Apr. 7, 1997, p. 2. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459, 5,434,872; 6,327,625; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition.) '872 patent at claim 15 ("…underrun control logic, which detects an underrun condition in which the host interface means in transferring data to the buffer memory falls behind the network interface means in transferring data to the transceiver, and means for supplying a bad frame signal to the communication media in response to the underrun condition.") '872 patent at claim 18 (…underrun control means, coupled with the network interface means, for detecting an underrun condition in which the host interface means in downloading data to the transmit data buffer falls behind the network interface means in transferring data to the transceiver, and for supplying a bad frame signal to the network transceiver in response to the underrun condition.") '872 patent at claim 24 ("…underrun control logic, which detects a condition in which the data transfer circuitry falls behind the medium access controller, and supplies a bad frame signal to the network in response to the underrun condition.") '094 patent at claim 4 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the network; and supplying a bad frame signal to the network un response to the underrun condition.") '094 patent at claim 16 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the communications medium; and supplying a bad frame signal to the communications medium in response to the underrun condition.")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		'094 patent at claim 34 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the network transceiver; and supplying a bad frame signal to the network transceiver in response to the underrun condition.") '094 patent at claim 41 ("…detecting an underrun condition in which the transfer of the data of the frame into the buffer memory falls behind the transmission of the data from the buffer memory to the network; and supplying a bad frame signal to the network in response to the underrun condition.") Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.
"**altering** the threshold" found in claim numbers: '094 patent: 47	PROPOSED CONSTRUCTION: changing DICTIONARY/TREATISE DEFINITIONS: See "**alterable storage location**" in subsection 1 for definitions of "alter" and "**optimizing the threshold**" in subsection 2 for definitions of "threshold." INTRINSIC EVIDENCE: Claims: see, e.g., claim 49 ("including allowing alteration of the threshold value while data of a frame to be transmitted is stored in the buffer memory"); see also claim 47; claim 48; claim 50; claim 51; claim 53; Specification: see, e.g., figs. 2, 4, 13, 14, 17, 18; col. 4:38-39 ("The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30"); col. 4:43-46 ("In yet other alternatives, the threshold store may be implemented using user specified data in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices."); see also col. 2:23-26; col. 4:38-41; col. 28:1-17; col. 4:38-46; col. 2:21-27; col. 27:44-28:17; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 55; Specification as Filed, p. 58. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459, 5,434,872; 6,327,625; 6,526,446; and 6,570,884.	PROPOSED CONSTRUCTION: dynamically changing INTRINSIC EVIDENCE: '094 patent, Abstract ("The monitoring logic includes a threshold store, which is *programmable by the host computer* for storing a threshold value. Thus, *the threshold value may be set by the host system to optimize performance in a given setting*.") '094 patent at 4:38-46 ("*The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30*. In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31. *Alternatively, the threshold store may be a read only memory set during manufacture*. In yet other alternatives, the threshold store may be implemented using user specified data in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices.") '094 patent at 2: 21-27 ("In one aspect of the invention, *the monitoring logic includes a threshold store, which is programmable by the host computer* for storing a threshold value and logic for posting status information to the host. Thus, *the threshold*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	*value may be set by the host system to optimize performance using the alterable threshold store* and the posted status information.") '094 patent at 27:44-28:17 ("XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, . . . , before the adapter can commence with the media access control functions associated with transmitting the frame. . . . The value for this register *may be programmed by the host to optimize performance*. If set too low, system latencies or bandwidth limitations may cause the adapter to underrun the network during transmission, causing a partial frame with a guaranteed bad CRC to be transmitted. If the value is set too high, then unnecessary delays will be incurred before the start of transmission. . . .") DICTIONARY/TREATISE DEFINITIONS: Webster's Ninth New Collegiate Dictionary (Ninth Edition, 1988) Alter: 1: to make different without changing into something else 2: CASTRATE SPAY ~ vi: to become different syn see CHANGE; alterable – adj. The American Heritage Dictionary of the English Language (4th Ed. 2000) alter: v. tr. To change or make different; modify: altered my will. intr. To change or become different. threshold Webster's Ninth New Collegiate Dictionary (1983) Threshold - A level, point, or value above which something is true or will take place and below which it is not or will not. The American Heritage Dictionary of the English Language (4th ed. 2000) The point that must be exceeded to begin producing a given effect or result or to elicit a response. McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold: 1. The least value of a current, voltage, or other quantity that produces the

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		minimum detectable response. It is also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation. Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.

4. U.S. Pat. No. 6,327,625

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**buffer**" found in claim numbers: '625 patent: 23	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 15 ("15. A method for managing transfer of data packets between a host processor and a network, comprising: storing packets in a first-in-first-out buffer in an order of receipt; identifying packets as having respective packet types from a plurality of packet types; and transferring packets out of the first-in-a first-out buffer according to the order of receipt, and according to the packet type so that packets having a particular packet type are transferred out of the order of receipt relative to packets having another packet type."); claim 18 (same); claim 19 (same); claim 21 (same); claim 22 (same); see also claim 1; claim 2; claim 3; claim 6; claim 7; claim 8; claim 9; claim 10; claim 11; claim 12; claim 13; claim 15,	PROPOSED CONSTRUCTION: A First-In-First-Out or "FIFO" storage device. DICTIONARY/TREATISE DEFINITIONS: Newton's Telecom: "**Buffer** 1. In data transmission, a buffer is a temporary storage location for information being sent or received." "**FIFO** First In, first Out. . . . FIFO . . . is a term used in data communications. It is a buffering scheme in which the first byte of data that enters the buffer is also the first byte retrieved by the CPU. This scheme is used. . . because it closely mimics the way serial data is actually transmitted; that is, one bit at a time." INTRINSIC EVIDENCE: '625 patent, col. 1, lines 13-67 ("[N]etwork interfaces are typically based on a first-in-first-out (FIFO) buffer. … The FIFO structure in network interface cards suffers the disadvantage that [it] supports only sequential data transfer. Each packet being loaded will be unloaded through the same sequence determined by the	Realtek agrees that the ordinary meaning of buffer is "a memory for temporary storage of data." However, Realtek reserves the right to rely on the proposed construction or any statement made by any party under the Patent Local Rules.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	claim 18, claim 19, claim 21, claim 22, claim 23; claim 24; claim 25; claim 28; claim 29; claim 30; claim 31; claim 33; claim 34; claim 35; Specification: see, e.g., col. 1:14-15 ("These network interfaces are typically based on a first-in-first-out (FIFO) buffer."); see also figs. 1-8; col. 1:13-67; col. 3:17-35; col. 3:64-67; col. 4:1-9; col. 4:40-5:7; col. 5:8-12:48; col. 9:47-50; col. 12:49-13:8; col. 13:23-53; col. 2:5 – 3:12; col. 3:17 -19; col. 3:29-33; col. 3:45-46; col. 3:61-67; col. 4:32-38; col. 4:40-43; col. 4:46-47; col. 4:53-54; col. 4:58-61; col. 5:4-7; col. 5:10-12; col. 5:35-36; col. 5:42-47; col. 5:64-66; col. 6:26-29; col. 7:6-8; col. 7:15-17; col. 7:20-23; col. 8:1-4; col. 11:58-67; col. 12:49-50; col. 13:39-42; col. 13:48-53; see also Prosecution History: Office Action, Feb. 2, 2001, p. 3; Office Action, Feb. 2, 2001, p. 4; Response to Office Action, May 1, 2001, p. 17-18; Response to Office Action, May 1, 2001, p. 19. EXTRINSIC EVIDENCE: See section I.A, supra (agreed upon definition for "buffer" in '884 patent); See also U.S. Patent Nos. 5,307,459, 5,434,872; 5,732,094; 6,526,446; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the	order of receipt of the packet. … The present invention supports … out of order processing of certain packets in the FIFO. In this manner, the optimized character of FIFO for sequential transfer is maintained, while particular types of packets are processed out of order to achieve minimum latency and maximum data security in an intelligent network interface card."); '625 patent, col. 3, lines 17-35 ("The present invention improves network interfaces based on FIFO buffer structures. … Priority packets can be transmitted or uploaded prior to normal packet traffic. … Furthermore, normal packets, priority packets and IPSec packets can coexist in a FIFO-based structure."); '625 patent, col. 3:64-67 ("FIG. 1 provides a conceptual diagram of an integrated circuit 10 including the logic for transferring data packets into and out of a FIFO buffer according to the present invention."); '625 patent, col. 4:1-9, Fig. 1 ("FIFO 13"); '625 patent, col. 4:40-5:7, Fig. 2 (describing data structure of FIFO 13); '625 patent, col. 5:8-12:48, Figs. 3-7 (describing circuitry associated with FIFO 13); '625 patent, col. 9:47-50 ("Thus, according to this embodiment of the present invention, normal packets [and] priority packets can be supported in a single FIFO structure with out of order packet transfer logic."); '625 patent, col. 12:49-13:8	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	(describing exemplary "single port memory [that] can be used for the FIFO packet buffer" shown in Fig. 1); '625 patent, col. 13:23-53, Fig. 8 (describing "network interface card 813" including "transmit FIFO buffer 822" and "receive FIFO buffer 826"); '625 patent, claim 15 ("A method for managing transfer of data packets between a host processor and a network, comprising: storing packets in a first-in-first-out buffer in an order of receipt…."); '625 patent, claim 18 (same); '625 patent, claim 19 (same); '625 patent, claim 21 (same); '625 patent, claim 22 (same); '625 patent, claim 23 ("a buffer . . . which stores data packets . . . in an order of receipt."); Prosecution History at DLINK 015386 (Response to First Official Action, dated May 1, 2001, p. 18)("[T]he citation within the James reference upon which the examiner relies does not identify a FIFO buffer.");Patents of Record, including U.S. Patent No. 5,212,778, col. 4:30-5:50, 7:30-57, 8:55-65, Figs. 1-5; U.S. Patent No. 5,828,835, Abstract, Col. 2:36-3:15, 10:34-11:20, 13:51-14:39, Figs. 8 and 13, Claims 1-4; see also U.S. Patent Nos. 4,783,730, 5,987,113, 6,138,189, 6,226,680. EXTRINSIC EVIDENCE: Testimony of Dr. Doshi	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		which will be based upon the intrinsic and extrinsic evidence cited above, as well as his knowledge of the usage of the term in the relevant art at the time the patent was filed. Dr. Doshi may also comment on the applicability of evidence cited by 3Com in support of its construction for this term. Transcript of February 5, 2006 Deposition of Li-Jau Yang at 48:21-55:1 ("It would be one FIFO, versus multiple queues"); Ex. 5, p. DLINK 015320; 71:1-74:24; Ex. 6, pp.3COM016060-61, 66. Transcript of February 1, 2006 Deposition Patricia C. Cross at 20:13-21:22; Ex. 1, pp. 3COM0097931-933; 3COM0097944-945, 966-967. D-Link reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. D-Link reserves the right to cite to any evidence cited by any party and to rely on any position taken by the parties under the Patent Local Rules.	

5. U.S. Pat. No. 6,526,446

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**data download circuit**" found in claim numbers: '446 patent: 26	PROPOSED CONSTRUCTION: A circuit that retrieves data from memory DICTIONARY/TREATISE DEFINITIONS: data: Dictionary of Computing (1st ed. 1983): Information that has been prepared, often in a particular format, for a specific purpose; see also Microsoft Computer Dictionary (5th ed. 2002): Plural of the	PROPOSED CONSTRUCTION: The circuitry that downloads data corresponding to the frame segment descriptor. INTRINSIC EVIDENCE: '446 patent at 8:28-38 ("With reference still to FIG. 2, *data download DMA circuit 212 utilizes the descriptors to retrieve and*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Latin datum, meaning an item of information; Dictionary of Computing (3d ed. 1990): Information that has been prepared, often in a particularly format, for a specific purpose; Webster's New World Computer Dictionary (10th ed. 2003): Factual information (such as text, numbers, sounds, and images) in a form that can be processed by a computer. McGraw-Hill Illustrated Telecom Dictionary (2d ed. 2000): In the communications industry, data is anything that is transmitted or processed digitally; download: The American Heritage Dictionary of the English Language (4th ed. 2000): To transfer (data or programs) from a server or host computer to one's own computer or device; circuit: The American Heritage Dictionary of the English Language (4th ed. 2000): The combination of a number of electrical devices and conductors that, when interconnected to a form a conducting path, fulfill some desired function; see also Dictionary of Computing (1st ed. 1983): Circuit: 1. The combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function. 2. A physical (electrical) connection used for communication. Dictionary of Computing (3d ed. 1990): Circuit: The combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function. INTRINSIC EVIDENCE: Claims: see, e.g., claim 1 ("A circuit for implementing transmission control protocol segmentation, said circuit comprising: a segmentation circuit coupled to receive a descriptor from a host device which corresponds to data, said segmentation circuit utilizes said descriptor to generate a frame segment descriptor; a data download circuit coupled to said segmentation circuit to receive said frame segment descriptor, said data download circuit retrieves said data from a memory; and a medium access control circuit coupled to said data download circuit to receive said data in a frame segment."); claim 14 ("said data download circuit comprises a data download direct memory access circuit");	*download the data file*, TCP templates, IP templates, and frame header stored within host memory 106. . . . *In other words, data download DMA circuit 212 receives the descriptor information from hardware queue 210 and uses it to retrieve the actual data stored within host memory 106.*") '446 patent, Abstract ("Hardware only transmission control protocol segmentation for a high performance network interface card. Specifically, one embodiment of the present invention includes a circuit for implementing transmission control protocol (TCP) segmentation. The circuit includes a segmentation circuit coupled to receive a descriptor from a host device which corresponds to data. *The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment. Furthermore, the circuit also includes a data download circuit coupled to the segmentation circuit to receive the frame segment descriptors. Specifically, the data download circuit retrieves the data from a memory.* Moreover, *the circuit includes a medium access control circuit coupled to the data download circuit to receive the data in a frame segment.*") '446 patent, Fig. 2 (showing Host Driver 202, Descriptor DMA 204, Segmentation State Machine 208, Hardware Queue 210, Data Download DMA 212, etc.) '446 patent, Fig. 4 ("receiving from a host device a descriptor signal corresponding to data stored within memory; *using the descriptor signal to generate a frame segment descriptor; receiving the data from the memory using a data download circuit*, etc.) DICTIONARY/TREATISE DEFINITIONS: circuit Newton's Telecom Dictionary (eleventh ed., 1996) Circuit: The physical connection (or path) of channels, conductors and equipment between two given points through which an electric current may be established. Includes both sending and receiving capabilities. A circuit can also be a network of circuit elements, such as resistors, inductors,

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	see also claim 4; claim 8; claim 15; claim 16; claim 18; claim 25; claim 26; Specification: Fig. 2; Fig. 4; col. 2:29-34; col. 2:52-57; col. 2:54-67; col. 8:28-38. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459, 5,434,872; 5,732,094; 6,327,625; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	capacitors, semiconductors, etc., that performs a specific function. A circuit can also be a closed path through which current can flow. The American Heritage Dictionary of the English Language (4th ed. 2000) The combination of a number of electrical devices and conductors that, when interconnected to a form a conducting path, fulfill some desired function. download The American Heritage Dictionary of the English Language (4th ed. 2000) To transfer (data or programs) from a server or host computer to one's own computer or device. Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules. EXTRINSIC EVIDENCE: Inventor Testimony of Li-Jau Yang (2/5/06): "Q. Looking down around line 58, it says, "In step 406 of figure 4, within the present embodiment, a data download circuit receives the data from the memory. It should be appreciated that the data download circuit uses the frame segment descriptor to retrieve the data from memory." What's a data download circuit? MR. STERN: Objection; foundation, competency. The document speaks for itself. THE WITNESS: It -- it is a DMA download logic. BY MS. RADER: Q. This is DMA logic? A. Right. Q. DMA download logic. And how does the DMA download logic use the frame segment descriptor to retrieve the data from memory? MR. STERN: Same objections. THE WITNESS: If you could -- it would use the pointer, as you already mentioned earlier, to retrieve the data from the host memory. BY MS. RADER: Q. So does the frame segment descriptor tell it the location in the host memory to go to find the data? Is that right? MR. STERN: Same objections; objection to the characterization. THE WITNESS: In this particular application, and based on what I've read so far, yes.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**a descriptor signal which corresponds to data stored within memory**" found in claim numbers: '446 patent: 26	PROPOSED CONSTRUCTION: A descriptor signal which describes data stored within host memory. DICTIONARY/TREATISE DEFINITIONS: See "**indication signal**" in subsection 1 for definitions of "signal," "**buffer memory**" in subsection 1 for definitions of "memory," and "**data download circuit**" in this subsection for definitions of "data"; descriptor: The American Heritage Dictionary of the English Language (4th ed. 2000): A word, phrase, or alphanumeric character used to identify an item in an information storage and retrieval system; Dictionary of Computing (1st ed. 1983): Stored information that describes how other information is stored, e.g. in an array, record, or file. By referring to the descriptor, a program can interpret the other data; IBM Dictionary of Computing (10th ed. 1993): A word or phrase used to categorize or index information; Microsoft Computer Dictionary (5th ed. 2002): In programming, a piece of stored information used to describe something else, often in terms of structure, content, or some other property; Dictionary of Computing (3d ed. 1990): Stored information that describes how other information is stored, e.g. in an array, record, or file. By referring to the descriptor, a program can interpret the other data; correspond: The American Heritage Dictionary of the English Language (4th ed. 2000): To be in agreement, harmony, or conformity. To be similar or equivalent in character, quantity, origin, structure, or function: English navel corresponds to Greek omphalos. See Synonyms at agree. To communicate by letter, usually over a period of time; INTRINSIC EVIDENCE: Claims: claim 1; claim 26; Specification: see, e.g., figs. 2-5; col. 2:43-46 ("the circuit includes a retriever circuit coupled to receive the first signal from the host device which indicates where a descriptor is located within the host memory. The retriever circuit also retrieves the descriptor which describes data stored within the host	PROPOSED CONSTRUCTION: A signal indicating where the corresponding data is in the host memory. INTRINSIC EVIDENCE: '446 patent at 5:66-6:6 ("Referring to FIG. 2, *a host driver 202* running on processor 106 of host system 100 *is responsible for creating a descriptor for a data file stored within host memory* 106 which is to be eventually transferred by network interface card (NIC) 118 over network 120. *The descriptor includes information about where the data file is stored within host memory 106*, the size of the data file, along with other information.") '446 patent at 6:19-22 ("*More specifically, the descriptor structure prepared by host driver 202 consists of* control words, *fragment address*, and fragment length. The control words contain packet related information and flags.") '446 patent, Abstract ("Hardware only transmission control protocol segmentation for a high performance network interface card. . . . The circuit includes a segmentation circuit coupled *to receive a descriptor from a host device which corresponds to data.* The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment. . . .") Fig. 4 (showing separate steps, including "receiving from a host device *a descriptor signal corresponding to data stored within memory*") DICTIONARY/TREATISE DEFINITIONS: Dictionary of Computing (3d ed. 1990): Stored information that describes how other information is stored, e.g. in an array, record, or file. By referring to the descriptor, a program can interpret the other data. The American Heritage Dictionary of the English Language (4th edition, 2000) A word, phrase, or alphanumeric character used to identify an item in an information storage and retrieval system.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	memory."); see also col. 2:25-42; col. 2:47-62; col. 5:66-6:32; 6:19-22; col. 6:51-55; col. 10:40-42. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459, 5,434,872; 5,732,094; 6,327,625; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	IBM Dictionary of Computing (10th ed. 1993): A word or phrase used to categorize or index information. Realtek reserves the right to rely on any statement made by any party unde ETRINSIC EVIDENCE: Inventor Testimony of Li-Jau Yang (2/5/06): "Q. Okay. So what's your understanding of the phrase that I just referred to, which is "a descriptor signal corresponding to data stored within memory"? MR. STERN: Objection; competency, foundation, asked and answered, calls for opinion testimony, and the document speaks for itself. THE WITNESS: That descriptor is the entry written into the queue. And as -- as a -- as a result of that write operation, that will make the FIFO not empty. And that -- that descriptor signal is pretty much stand for if FIFO is empty or not. So I hope this clarification ends all the questioning you have. BY MR. YANG: Q. Okay. And I hope the same, too. But let me just clarify a little bit. So you're saying that the descriptor signal we have been talking about is a status indication of the FIFO? A. That's correct." Yang Depo. Tr. (2/5/06) at 233:18-234:12. "Q. Okay. So that signal itself, which is the descriptor signal and which is also a 0 and 1, doesn't have -- doesn't have any other information other than a 0 or 1? A. That's correct." Yang Depo. Tr. (2/5/06) at 239:17-21.
"**frame segment descriptor**" found in claim numbers: '446 patent: 26	PROPOSED CONSTRUCTION: A descriptor for a frame segment. INTRINSIC EVIDENCE: Claims: claim 1; claim 4; claim 10; claim 11; claim 15; claim 16; claim 20; claim 21; claim 31; claim 32; claim 33; Specification: figs. 2-5; col. 2:29-31 ("the segmentation circuit utilizes the descriptor to generate	PROPOSED CONSTRUCTION: A descriptor identifying where the corresponding frame segment is in the host memory. INTRINSIC EVIDENCE: '446 patent at 6:58-7:14 ("Conversely, if the data file needs TCP segmentation, *TCP segmentation state machine 208 creates*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	other descriptors that describe each frame segment."); Fig. 4; col. 1:44-46; col. 2:27-37; col. 2:50-54; col. 2:63-65; col. 3:17-21; col. 3:23-26; col. 6:28-29; col. 6:63-67; col. 6:58-7:14; col. 7:5-8; col. 7:10-13; col. 7:28-31; col. 7:44-48; col. 7:48-50; col. 7:50-52; col. 7:52-54; col. 7:54-56; col. 7:58-60; col. 7:60-63; col. 7-8:66-3; col. 8:6-8; col. 8:8-10; col. 8:29-32; col. 8:45-47; col. 8:47-52; col. 8:52-54; col. 8:54-62; col. 8:62-66; col. 8-9:68-3; col. 9:3-5; col. 9:29-30; col. 9:30-32; col. 9:32-33; col. 9:33-35; col. 9:58-61; col. 9-10:64-2; col. 10:2-4; col. 10:6-9; col. 10:15-18; col. 10:18-20; col. 10:20-24; col. 10:44-57; col. 11:1-4; col. 11:34-36; col. 11:36-38; col. 11:40-42; col. 11:51-55. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459, 5,434,872; 5,732,094; 6,327,625; and 6,570,884. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	*another set of descriptors wherein each descriptor describes a fragment or a segment of the data file*. In other words, the data file stored within host memory 106 is virtually segmented down into a number of *frames. Within the present embodiment, each of the descriptors created by TCP segmentation state machine 208 is going to contain a pointer to a location in host memory 106* where a reusable "template" for the IP header is stored. Furthermore, each descriptors is also going to contain a pointer to a location in host memory 106 where a reusable "template" for the TCP header is stored. *Additionally, each of the descriptors would also include* a control word along with *pointers to where the data file (payload) is stored within host memory 106*. Also, each descriptor *contains a pointer to a location in host memory 106 where a reusable template* for the Medium Access Control (MAC) header *is stored*. These descriptors are then transmitted by TCP segmentation state machine 208 to hardware queue 210 for temporary storage. . . . As such, TCP segmentation state machine 208 transmits the revised structure descriptors to hardware queue 210 where they are temporarily stored. *This revised structure descriptor information stored within hardware queue 210 will subsequently be used by data download DMA circuit 212 to transfer data.*") '446 patent, Abstract ("Hardware only transmission control protocol segmentation for a high performance network interface card. Specifically, one embodiment of the present invention includes a circuit for implementing transmission control protocol (TCP) segmentation. The circuit includes a segmentation circuit coupled to receive a descriptor from a host device which corresponds to data. *The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment. Furthermore, the circuit also includes a data download circuit coupled to the segmentation circuit to receive the frame segment descriptors*. Specifically, the data download circuit retrieves the data from a memory. Moreover, the circuit includes a medium access control circuit

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		coupled to the data download circuit *to receive the data in a frame segment.* ") '446 patent, Fig. 4 ("receiving from a host device a descriptor signal corresponding to data stored within memory; *using the descriptor signal to generate a frame segment descriptor; receiving the data from the memory using a data download circuit*, etc.) '446 patent at 2: 27-37 ("The circuit includes a segmentation circuit coupled to receive a descriptor from a host device which corresponds to data. *The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment.* Furthermore, the circuit also includes *a data download circuit coupled to the segmentation circuit to receive the frame segment descriptors.* Specifically, the data download circuit retrieves the data from a memory. Moreover, the circuit includes a medium access control circuit coupled to the data download circuit *to receive the data in a frame segment.*") Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules. EXTRINSIC EVIDENCE: Inventor Testimony of Li-Jau Yang (2/5/06): "Q. And the reason why the data download circuit use the frame segment descriptor is because the frame segment descriptor indicates where the corresponding frame segment is stored in the host memory, correct? MR. STERN: Same objections. THE WITNESS: Yes." Yang Depo Tr. (2/5/06) at 243:4-10.

6. U.S. Pat. No. 6,570,884

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**a buffer, coupled to the first port, storing received packets**" found in claim	PROPOSED CONSTRUCTION: A temporary storage device connected to the first port for received packets.	PROPOSED CONSTRUCTION: A temporary storage device connected to the first port that is of sufficient size to store a plurality of received	Realtek agrees that the ordinary meaning of buffer is "a memory for temporary storage of data." However, Realtek reserves the right to

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
numbers: '884 patent: 1	DICTIONARY/TREATISE DEFINITIONS: See "**buffer**," in subsection 1 for definitions of that term and Part I.A for the agreed upon definition of "**port**"; store: The American Heritage Dictionary of the English Language (4th Ed. 2000): v. Computer Science. To copy (data) into memory or onto a storage device, such as a hard disk. INTRINSIC EVIDENCE: Claims: see, e.g., claim 3 (3: "The interface of claim 2, wherein the buffer includes memory for a plurality of packets having a typical size."); claim 23 ("23: The interface of claim 21, wherein the buffer includes memory for a plurality of packets having a typical size."); see also claim 1; claim 13; claim 16; claim 21; claim 22; claim 40; Specification: see, e.g., col. 3:11-29; col. 4:61-65, Fig. 2; col. 5:38-42, Fig. 3; col. 6:38-42; col. 6:58-7:34, Fig. 5; col. 8:63-9:27; col. 10:23-29; see also Prosecution History: Response to Office Action, May 14, 2001, p. 2; Response to Office Action, May 14, 2001, p. 6; Response to Office Action, Oct. 26, 2001, p. 2; Final Office Action, Mar. 20, 2002, p. 7; Final Office Action, Mar. 20, 2002, p. 8; RCE and Amendment, Aug. 15, 2002, pp. 10-12; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 13-14; Notice of Allowance, Feb. 2, 2003, p. 2. EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459,	packets. DICTIONARY/TREATISE DEFINITIONS: Newton's Telecom: "**Buffer** 1. In data transmission, a buffer is a temporary storage location for information being sent or received." "**Packet Buffer** Memory set aside for storing a packet awaiting transmission or for storing a received packet." INTRINSIC EVIDENCE: '884 patent col. 1:66-2:16 ("In particular, the present invention provides an interface that comprises the first port on which incoming data is received at the data transfer rate of the network, a buffer coupled to the port that stores received packets, and a second port coupled with the buffer through which transfer of packets to the host is executed. Packet filters are coupled to the first port which identifies packets being stored in the buffer that have one of the plurality of variant formats. A processor is coupled with the buffer as well, and is responsive to the packet filter to process identified packets in the buffer. In this manner, the processor is able to operate at a slower speed, such that the processing time for a typical packet is greater than the amount of time that is consumed by storing a typical packet in the buffer. Because the processor is only required to handle packets identified by the dedicated packet filter logic, it need not have the capability to keep up with	rely on any proposed construction or any statement made by any party under the Patent Local Rules.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	5,434,872; 5,732,094; 6,327,625; and 6,526,446. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	the entire data stream."); '884 patent col. 3:11-29 (" When a particular packet in the FIFO buffer reaches a stage for upload to the host computer, the logic on the network interface card issues an interrupt to the processor on the network interface card if a flag is set. In response to the interrupt, the packet in the FIFO buffer is processed locally on the network interface card. If the FIFO buffer overflows during the processing of the packet, then packets may be lost. However, because of the relatively small number of packets to be processed by the local processor, very few packets will be lost in the typical network."); '884 patent col. 4:61-65, Fig. 2; '884 patent col. 5:38-42, Fig. 3; '884 patent col. 6:38-42; '884 patent col. 6:58-7:34, Fig. 5 ("FIG. 5 illustrates the processing which occurs upon interrupting the processor, and the handling of the packet by the processor. The process begins when a packet is at the top of the receive FIFO by testing the packet header (block 400). The logic determines whether a pattern match bit is set (block 41). If the pattern match bit is set, then the processor is interrupted and the receive FIFO is stalled (block 402). Other incoming packets may still be stored in the FIFO, until it overflows. In a typical case, the processor is able to handle the packet, before a FIFO overflow condition occurs. ... Upon completion	

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		of processing, the FIFO is "un-stalled" to begin continued handling of the data flow (block 405). After restarting the FIFO, the process proceeds (block 406) with handling packets in the data stream. If the pattern match bit was not set a block 401, then the process branches to block 406 directly. Alternative implementations are possible here. For example, the system could issue an interrupt to the processor as soon as the match is detected, rather than waiting for the packet to get to the top of the FIFO. An immediate interrupt could result in more than one packet interrupting the processor and require some kind of stack or other control construct to specify where the corresponding packets were.") '884 patent col. 8:63-9:27 ("After examining the matched packet, the ARM7 processor can instruct the upload state machine to either transfer the packet to the host or to discard it. All packets behind the matched packet will not be uploaded to the host until the ARM7 processor has completely processed the matched packet. If the processor takes too long to process the matched packet, and other incoming packets continue to be received off the network, the overflow condition may occur in the receive FIFO and result in dropping incoming packets. The expectation is that this problem can be avoided under most reasonable network traffic conditions since most of the packets	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		the ARM7 processor needs to examine are short, and a block 2 K bytes of receive FIFO provides about 160 us at 100 Mbps for the processor to make the final decision."); '884 patent col. 10:23-29 ("To read the packet data, the ARM7 must determine where the start and end of the data is. The address of the first word of packet data for the packet at the top of the receive FIFO is contained in a pointer register associated with the FIFO. The end of the current packet is determined by reading another pointer register, which points to the first byte after the last valid byte in the packet at the top of the receive FIFO. The data in the FIFO can then be read.") EXTRINSIC EVIDENCE: Testimony of Dr. Doshi which will be based upon the intrinsic and extrinsic evidence cited above, as well as his knowledge of the usage of the term in the relevant art at the time the patent was filed. Dr. Doshi may also comment on the applicability of evidence cited by 3Com in support of its construction for this term. Transcript of February 1, 2006 Deposition Patricia C. Cross at 20:13-46:18; 60:22-61:13; 65:4-65:24; 115:7-13; Ex. 1, pp. 3COM0097931-938; Ex. 3, pp. 3COM016497-498, 500, 504-506; Ex. 4, pp. 3COM0079064-068, 112-120. D-Link reserves the right to	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		rely on any testimony or exhibit therein made or introduced during the course of any deposition. D-Link reserves the right to cite to any evidence cited by any party and to rely on any position taken by the parties under the Patent Local Rules.	
"read and process data in the identified packets **from the buffer**" found in claim numbers: '884 patent: 1	PROPOSED CONSTRUCTION: from the buffer DICTIONARY/TREATISE DEFINITIONS: See "**buffer**," in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 13 ("logic which signals the second logic to process the data after at least part of the identified packet is stored in the buffer"); claim 14 ("logic which signals the second logic to process the data after the identified packet is stored in the buffer"); see also claims 1-12; claims 14-15; claim 21; claim 40; Specification: figs. 1-5; col. 6:38-40 ("In an alternative embodiment, the packet is supplied in parallel to a RAM buffer which is independent of the receive FIFO"); Fig. 5; 6:36-37; 3:19-26; 6:58-7:7; 10:22-29; 10:35-38; see also Prosecution History: Amendment, October 26, 2001, p. 2; RCE and Amendment, Aug. 15, 2002, p. 7; RCE and Amendment, Aug. 15, 2002, p. 11; RCE and Amendment, Aug. 15, 2002, p. 12; Response to Office Action, Jan. 22, 2003, p. 8; Response to Office Action, Jan. 22, 2003, p. 13-14; Notice of Allowance, Feb. 2, 2003, p. 2.	PROPOSED CONSTRUCTION: while the packets are in the buffer INTRINSIC EVIDENCE: '884 patent col. 6:36-37; Fig. 3 ("The processor accesses the packet from the receive FIFO 201 for processing."); '884 patent at 3:19-26 ("When a particular packet in the FIFO buffer reaches a stage for upload to the host computer, the logic on the network interface card issues an interrupt to the processor on the network interface card if a flag is set. In response to the interrupt, the packet in the FIFO buffer is processed locally on the network interface card. If the FIFO buffer overflows during the processing of the packet, then packets may be lost."); '884 patent col. 6:58-7:7; Fig. 5 ("If the pattern match bit is set, then the processor is interrupted and the receive FIFO is stalled (block 402). … Upon receiving the interrupt, the processor handles the packet (block 403). As result of the packet handling process, the processor decides whether to discard the packet, modify the packet, or do nothing allowing the packet to proceed unchanged to the host	PROPOSED CONSTRUCTION: while the packets are in the buffer INTRINSIC EVIDENCE: '884 patent at 6:36-37 ("*The processor accesses the packet from the receive FIFO 201 for processing.*") '884 File History, Bates No. 3COM11713, lines 6-8 ("The present invention is directed to a network interface which *has logic to process packets in the frame buffer* that are identified by a packet filter as having a particular format, *before the packets are transferred* to the host processor to which they are addressed.") '884 patent at 3:19-26 ("When a particular packet in the FIFO buffer reaches a stage for upload to the host computer, the logic on the network interface card issues an interrupt to the processor on the network interface card if a flag is set. *In response to the interrupt, the packet in the FIFO buffer is processed locally on the network interface card.* If the FIFO buffer overflows during the processing of the packet, then packets may be lost.") '884 patent at 6:58-7:7; Fig.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	EXTRINSIC EVIDENCE: U.S. Patent Nos. 5,307,459, 5,434,872; 5,732,094; 6,327,625; and 6,526,446. 3Com reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. 3Com reserves the right to cite to any evidence cited by any party and reserves the right to rely on any document or statement made by any party under the Patent Local Rules. 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	(block 404)."); '884 patent col. 8:67-9:24 ("Once the packet advances to the front of the FIFO, an interrupt is generated to the ARM7 processor specifying that a packet pattern match has occurred and which engine has the match. The ARM7 processor reads a read pointer register, which controls the receive FIFO upload operation, for the starting address of the matched packet in the receive FIFO. During the processing of the matched packet, the ARM7 processor has a limited amount of time to decide what to do with the matched packet …. All packets behind the matched packet will not be uploaded to the host until the ARM7 processor has completely processed the matched packet. If the processor takes too long to process the matched packet, and other incoming packets continue to be received off the network, the overflow condition may occur in the receive FIFO and result in dropping incoming packets. The expectation is that this problem can be avoided under most reasonable network traffic conditions since most of the packets the ARM7 processor needs to examine are short, and a block 2 K bytes of receive FIFO provides about 160 us at 100 Mbps for the processor to make the final decision."); '884 patent col. 10:22-29 ("To read the packet data, the ARM7 must determine where the start and end of the data is. The address of the first word of packet data for the packet at the top of	5 ("FIG. 5 illustrates the processing which occurs upon interrupting the processor, and the handling of the packet by the processor. *The process begins when a packet is at the top of the receive FIFO* by testing the packet header (block 400). The logic determines whether a pattern match bit is set (block 41). *If the pattern match bit is set, then the processor is interrupted and the receive FIFO is stalled (block 402)*. . . . Upon receiving the interrupt, the processor handles the packet (block 403). . . . Upon completion of processing, *the FIFO is "un-stalled" to begin continued handling of the data flow (block 405)*.") '884 patent col. 10:22-29 ("To read the packet data, the ARM7 must determine where the start and end of the data is. The address of the first word of packet data for the packet at the top of the receive FIFO is contained in a pointer register associated with the FIFO. The end of the current packet is determined by reading another pointer register, which points to the first byte after the last valid byte in the packet at the top of the receive FIFO. The data in the FIFO can then be read.") ; '884 patent col. 10:35-38 ("When pattern matching is enabled, the ARM7 may wish to examine the contents of the packet which was matched. To do this it must read the data out of the receive FIFO."); Prosecution History at

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		the receive FIFO is contained in a pointer register associated with the FIFO. The end of the current packet is determined by reading another pointer register, which points to the first byte after the last valid byte in the packet at the top of the receive FIFO. The data in the FIFO can then be read.") ; '884 patent col. 10:35-38 ("When pattern matching is enabled, the ARM7 may wish to examine the contents of the packet which was matched. To do this it must read the data out of the receive FIFO."); Prosecution History at DLINK 015519 (Response to Second Official Action, dated October 26, 2001, p. 2) ("The present invention is directed to a network interface which has logic to process packets in the frame buffer that are identified by a packet filter as having a particular format, before the packets are transferred to the host processor to which they are addressed."). EXTRINSIC EVIDENCE: Testimony of Dr. Doshi which will be based upon the intrinsic and extrinsic evidence cited above, as well as his knowledge of the usage of the term in the relevant art at the time the patent was filed. Dr. Doshi may also comment on the applicability of evidence cited by 3Com in support of its construction for this term. Transcript of February 1, 2006 Deposition Patricia C. Cross at 20:13-46:18; 60:22-61:13; 65:4-65:24;	DLINK 015519 (Response to Second Official Action, dated October 26, 2001, p. 2) ("The present invention is directed to a network interface which has logic to process packets in the frame buffer that are identified by a packet filter as having a particular format, before the packets are transferred to the host processor to which they are addressed."). '884 File History, Bates No. 3COM11743 (Rule 1.121 Marked-Up Claims), lines 11-13 ("second logic coupled with the buffer, and responsive to the packet filter *to read and process data in the identified packets from the buffer*, and to produce a data value dependent on contents of the packet prior to transfer of the identified packets to the second port but the first logic.") (underline text added to the claim during the prosecution of the '884 patent.) '884 patent, Fig. 5 ("402 INTERRUPT PROCESSOR/STALL FIFO; 403 PROCESS PACKET; 404 DISCARD PARKET [sic], MODIFY PACKET, OR DO NOTHING TO PACKET; 404 "UN-STALL" FIFO"; 406 PROCEED) Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		115:7-13; Ex. 1, pp. 3COM0097931-938; Ex. 3, pp. 3COM016497-498, 500, 504-506; Ex. 4, pp. 3COM0079064-068, 112-120. D-Link reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. D-Link reserves the right to cite to any evidence cited by any party and to rely on any position taken by the parties under the Patent Local Rules.	

B. Claim Elements in Dispute as to Whether 35 U.S.C. § 112 ¶ 6 Applies

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
"**logic to transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types so that packets having a particular packet type are transferred out of the order of receipt, relative to packets having another packet type**" found in claim numbers: '625 patent: 23	3Com asserts that "logic" is a term of art that means "Circuitry and/or programming" rather than a term of claim drafting that invokes 35 U.S.C. § 112 ¶ 6. See "**transmit logic, responsive to the means . . . .**" supra for DICTIONARY/TREATISE DEFINITIONS and EXTRINSIC EVIDENCE supporting 3Com's construction of "logic." The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**packet filter 14**" (see fig. 1; col. 4, ln. 13); "**FIFO(s) 13**" (see fig. 1; col. 4, ln. 2-5, 14); "**frame start header 16**" (see fig. 1; col. 4, ln. 15); "**frame start header 17**" (see fig. 1; col. 4, ln. 18); "**top packet data 18**" (see fig. 1; col. 4, ln. 18); "**IPsec queue 20**" (see fig. 1; col. 4, ln. 21); "**priority queue 21**" (see fig. 1; col. 4, ln. 21-22); "**packet download/receive control block 22**" (see fig.	This claim element should be governed by 35 U.S.C. § 112 ¶6. The corresponding structure disclosed in the '625 patent consists of "**IPsec queue 20**" (fig. 1, col. 4:21), "**priority queue 21**" (fig. 1, col. 4:21-22), "**packet upload/transmit control logic 24**" (fig. 1, col. 4:26), "**out of order packet transfer control block 25**" (fig. 1, col. 4:28), "**logic 26**" (fig. 1, col. 4:29), "**logic 27**" (fig. 1, col. 4:30) , "**memory arbitration logic 28**" (fig. 1, col. 4:34-35), "**multiplexer 29**" (fig. 1, col. 4:35), "**packet transmit/upload logic 24**" (fig. 5, col. 7:16); **"idle state 200"** (fig. 5, col. 7:17-18); "**state 201**" (fig. 5; col. 7:19); "**path 202**" (fig. 5, col. 7:25); "**align pointer state 203**" (fig. 5, col. 7:25) "**branch 204**" (fig. 5, col. 7:25)**;** "**state 205**" (fig. 5, col. 7:26); "**data transfer state 206**" (fig. 5, col. 7:29); "**branch 207**" (fig. 5, col. 7:50)**;** "**retransmit state 208**" (fig. 5, col. 7:51)**;** "**branch 209**" (fig. 5, col. 7:55); "**flush state 210**" (fig. 5, col. 7:57); "**branch 211**" (fig. 5, col. 7:62); "**transfer complete state 212**" (fig. 5, col. 7:62-63); "**idle state 150**" (fig. 6, col. 8:52); "**branch 151**" (fig. 6, col. 8:55); "**transfer state 152**" (fig. 6, col. 8:58); "**state 153**" (fig. 6, col. 8:61); "**state 154**" (fig. 6, col. 8:62); "**path 155**" (fig.	Realtek does not dispute the applicability of 35 U.S.C. § 112 ¶6 to this claim element. However, Realtek identifies the following as the corresponding structure to the extent that the Court finds that 35 U.S.C. § 112 ¶ 6 governs this claim element. Fig. 1 – packet upload/transmit control 24, out of order packet transfer control 25, priority queue 21 Fig. 5 – elements 200, 201, 202, 203, 204, 205, and 206 Fig. 6 – elements 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 165, 167, 168, 169, 170, 171, 172, and 173Fig. 8 – ASIC 814, filters and processing resources 830, upload engine 825 Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	1; col. 4, ln. 22-23); "**IPsec packet processing resources 23**" (see fig. 1; col. 4, ln. 25); "**packet upload/transmit control logic 24**" (see fig. 1; col. 4, ln. 26); "**out of order packet transfer control block 25**" (see fig. 1; col. 4, ln. 28); "**logic 26**" (see fig. 1; col. 4, ln. 29); "**logic 27**" (see fig. 1; col. 4, ln. 30); "**memory arbitration logic 28**" (see fig. 1; col. 4, ln. 34-35); "**multiplexer 29**" (see fig. 1; col. 4, ln. 35); "**idle state 100**" (see fig. 3; col. 5, ln. 10); "**state 101**" (see fig. 3; col. 5, ln. 12); "**state 102**" (see fig. 3; col. 5, ln. 14); "**branch 103**" (see fig. 3; col. 5, ln. 20); "**branch 104**" (see fig. 3; col. 5, ln. 21); "**branch 105**" (see fig. 3; col. 5, ln. 22); "**state 106**" (see fig. 3; col. 5, ln. 24); "**state 107**" (see fig. 3; col. 5, ln. 29); "**state 108**" (see fig. 3; col. 5, ln. 32); "**state 120**" (see fig. 4; col. 6, ln. 32); "**state 121**" (see fig. 4; col. 6, ln. 38); "**state 122**" (see fig. 4; col. 6, ln. 46); "**state 123**" (see fig. 4; col. 6, ln. 49); "**state 124**" (see fig. 4; col. 6, ln. 54); "**packet transmit/upload logic 24**" (see fig. 5; col. 7, ln 16); "**idle state 200**" (see fig. 5; col. 7, ln 17-18); "**state 201**" (see fig. 5; col. 7, ln 19); "**path 202**" (see fig. 5; col. 7, ln 25); "**align pointer state 203**" (see fig. 5; col. 7, ln 25); "**branch 204**" (see fig. 5; col. 7, ln 25); "**state 205**" (see fig. 5; col. 7, ln 26); "**data**	6, col. 8:66), "**path 156**" (fig. 6, col. 9:3), "**path 157**" (fig. 6, col. 9:3), "**path 158**" (fig. 6, col. 9:3); "**state 160**" (fig. 6, col. 9:9); "**state 161**" (fig. 6, col. 9:14); "**state 165**" (fig. 6, col. 9:17); "**state 166**" (fig. 6, col. 9:18); "**state 167**" (fig. 6, col. 9:19); "**state 168**" (fig. 6, col. 9:24); "**state 169**" (fig. 6, col. 9:26); "**state 170**" (fig. 6, col. 9:27); "**path 171**" (fig. 6, col. 9:30); "**path 172**" (fig. 6, col. 9:31); "**restore pointer path 173**" (fig. 6, col. 9:31); and "**resources 830**" (fig. 8, col. 13:49).	

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	transfer state 206" (see fig. 5; col. 7, ln 29); "**branch 207**" (see fig. 5; col. 7, ln 50); "**retransmit state 208**" (see fig. 5; col. 7, ln 51); "**branch 209**" (see fig. 5; col. 7, ln 55); "**flush state 210**" (see fig. 5; col. 7, ln 57); "**branch 211**" (see fig. 5; col. 7, ln 62); "**transfer complete state 212**" (see fig. 5; col. 7, ln 62-63); and "**resources 830**" (see fig. 8; col. 13, ln. 48); see also elements 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 165, 167, 168, 169, 170, 171, 172, and 173 (fig. 6); ASIC 814, filters and processing resources 830, upload engine 825 (fig. 8).		
"**second logic coupled with the buffer, and responsive to the packet filter to read and process data in the identified packets from the buffer, and to produce a data value dependent on contents of the packet prior to transfer of the identified packets to the second port by the first logic**" found in claim numbers: '884 patent: 1	3Com asserts that "logic" is a term of art that means "Circuitry and/or programming" rather than a term of claim drafting that invokes 35 U.S.C. § 112 ¶ 6. See "**transmit logic, responsive to the means . . . .**" supra for DICTIONARY/TREATISE DEFINITIONS and EXTRINSIC EVIDENCE supporting 3Com's construction of "logic." The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. To the extent that the Court finds this element to be governed by 35 U.S.C. §	This claim element should be governed by 35 U.S.C. § 112 ¶6. The corresponding structure disclosed in the '884 patent consists of "**embedded processor 14**" (fig. 1, col. 4:14-15), "**embedded processor 118**" (fig. 2, col. 5:8), "**processor 220**" (fig. 3, col. 6:36), and "**ARM7 embedded processor subsystem**" (col. 5:14-21). See also Cols. 1:61-2:16; 3:47-56; 4:28-36; 5:8-21; 6:34-37; 6:58-7:11; 9:1-26; 10:11-43. In the alternative, in the event this phrase is determined not to be governed by 35 U.S.C. § 112 ¶6, D-Link believes the term "second logic" should be construed to mean "processing resources configured to perform specified binary tasks,	Realtek does not dispute the applicability of 35 U.S.C. § 112 ¶6 to this claim element. However, Realtek identifies the following as the corresponding structure to the extent that the Court finds that 35 U.S.C. § 112 ¶ 6 governs this claim element. Fig. 1 – processor (slower) 14 Fig. 2 – processor (slower than data path) 118, including ARM 7 processor Fig. 3 – processor 220 Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	112 ¶ 6, such "second logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**hardware filtering logic 15**" (see fig. 1; col. 4, ln. 16); "**embedded processor 14**" (see fig. 1; col. 4, ln. 15-16); "**line 18**" (see fig. 1; col. 4, ln. 26); "**embedded processor 118**" (see fig. 2; col. 5, ln. 8); "**pattern match modules, modules 203, 204, 205 and 206**" (see fig. 3; col. 5, ln. 43); "**packet classify unit 210**" (see fig. 3; col. 5, ln. 44); "**receive FIFO control logic 218**" (see fig. 3; col. 6, ln. 29); "**processor 220**" (see fig. 3; col. 6, ln. 36); "**block 300**" (see fig. 4; col. 6, ln. 45); "**block 301**" (see fig. 4; col. 6, ln. 47-48); "**block 302**" (see fig. 4; col. 6, ln. 49); "**block 303**" (see fig. 4; col. 6, ln. 50); "**block 304**" (see fig. 4; col. 6, ln. 52); "**block 305**" (see fig. 4; col. 6, ln. 54); "**block 306**" (see fig. 4; col. 6, ln. 55); "**block 400**" (see fig. 5; col. 6, ln. 61); "**block 41**" (see col. 6, ln. 63); "**block 401**" (see fig. 5); "**block 402**" (see fig. 5; col. 6, ln. 64); "**block 403**" (see fig. 5; col. 7, ln. 2); "**block 404**" (see fig. 5; col. 7, ln. 5); "**block 405**" (see fig. 5; col. 7, ln. 7); "**block 406**" (see fig. 5; col. 7, ln. 8); "**ARM7 processor**" (col. 9, ln. 23); and "**general purpose processor module**" (see col. 11, ln. 29).	where the processing resources operate at speeds slower than the speed of the incoming packet stream." INTRINSIC EVIDENCE: '884 patent col. 1:47-58 ("Relatively powerful processors by today's standards are required to keep up with fast networks, such as 100 Megabit per second or Gigabit per second Ethernet. However, such powerful processors add significant cost to the network interface cards. This imbalance in the cost of processing power and network speed is likely to continue to arise in a variety of settings as technology advances on both fronts. Accordingly, it is desirable to provide a network interface capable of handling certain specialized packets, without incurring the increased costs associated with powerful on chip, or on-board, processors."); '884 patent col. 1:61-2:16 ("The present invention provides a network interface card, or an interface to other types of communication channels, with limited intelligence, implemented using a relatively slower, and lower cost embedded processor, supported by dedicated hardware logic for the purposes of intercepting certain packets being received via the network. … Because the processor is only required to handle packets identified by the	

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		dedicated packet filter logic, it need not have the capability to keep up with the entire data stream."); '884 patent col. 3:47-53 ("Accordingly, an integrated circuit network interface device for a high speed network medium is provided with the relatively slow, low-cost embedded processor. Hardware pattern matching logic supports pattern matching at the speed of the incoming packet stream, and signals the embedded processor when a packet having one of the plurality of variant formats is detected."); '884 patent col. 4:28-36, Fig. 1 ("The integrated circuit 10 is capable therefore of handling higher speed networks with more complex network management functions, with reduced disruption of the processes in the receive path 13, with a lower cost processor. The processor 14 assisted by the hardware filter 15 may be slower, and have lower cost, than a more complex and higher speed processor which would be required without the filter 15."); '884 patent col. 5:8-21 ("An embedded processor 118 is also coupled to the receive path, and to other components on the ASIC 101. The embedded processor 118 is coupled to the on-board memory 103 via interface 119. The processor executes instructions stored in the	

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		memory 103, in order to process identified packets in the receive path. In one embodiment, the processor 118 comprises a RISC processor operating with a processor clock of 25 MHz, such as for example an ARM7 embedded processor subsystem commercially available from ARM Ltd., of Cambridge, England. The effective instruction execution rate of the processor in this example is less than 25 MHz, because of the limitations imposed by the speed of the on-board memory 103."); '884 patent col. 6:34-37 ("When a packet reaches the top of the receive FIFO 201, the receive FIFO control logic 218 generates an interrupt on line 219 to the processor 220. The processor accesses the packet from the receive FIFO 201 for processing."); '884 patent col. 6:58-7:11, Fig. 5 (describing "the handling of the packet by the processor"); '884 patent col. 9:1-26 (describing implementation with "ARM7 processor"); '884 patent col. 10:11-43 (same); '884 patent col. 10:53-58 ("The invention is also applicable to other environments, including environments … in which a communication channel is supplying data packets at a high-speed relative to the processing power used for handling selected packets in the channel.").	

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		EXTRINSIC EVIDENCE: Testimony of Dr. Doshi which will be based upon the intrinsic and extrinsic evidence cited above, as well as his knowledge of the usage of the term in the relevant art at the time the patent was filed. Dr. Doshi may also comment on the applicability of evidence cited by 3Com in support of its construction for this term. Transcript of February 1, 2006 Deposition Patricia C. Cross at 20:13-46:18; 60:22-61:13; 65:4-65:24; 115:7-13; Ex. 1, pp. 3COM0097931-938; Ex. 3, pp. 3COM016497-498, 500, 504-506; Ex. 4, pp. 3COM0079064-068, 112-120. D-Link reserves the right to rely on any testimony or exhibit therein made or introduced during the course of any deposition. D-Link reserves the right to cite to any evidence cited by any party and to rely on any position taken by the parties under the Patent Local Rules.	
"means for comparing the counter to the threshold value in the alterable storage location and **generating an indication signal to the host processor**	3Com agrees that 35 U.S.C. § 112 ¶ 6 governs "**means for comparing**" but does not govern the additional limitation of "generating." To the extent the Court finds § 112 ¶ 6 applicable to "generating," each of the following structures, acts or materials, without	.	Realtek contends that 35 U.S.C. § 112 ¶ 6 governs both "means for comparing . . ." and "means for . . . generating an indication signal . . . ." and identifies the corresponding structures, acts, or materials as follows:

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
responsive to a comparison of the counter and the alterable storage location" found in claim numbers: '459 patent: 1	limitation, which correspond to "means for comparing" are also enabling with respect to the generation of an indication signal to a host processor: "**comparator 213**" outputs data to "**RCV COMPLETE control block 210**" (see fig. 14, col. 31, ln. 41), which generates an indication signal (see col 31, ln. 41-49); "**EARLY INDICATION LATCH block 512**" (see col. 38, ln. 51-55); "**early xmit complete block**" (see col. 39, ln 57); and "**AND gate 616**" (see fig. 31; col. 40, ln. 46); see also receive threshold logic (figs. 12a-18); transfer threshold logic (figs. 19-23); download transmit threshold logic (figs. 24-28); transmit threshold logic (figs. 29-34).		Figs. 12a-18 – receive threshold logic Figs. 19-23 – transfer threshold logic Figs 24-28 – download transmit threshold logic Figs. 29-34 – transmit threshold logic Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.
"means**, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value,** for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory" found in claim	3Com contends that the means for monitoring the transferring of data is governed by 35 U.S.C. § 112 ¶ 6, but contends that the buffer memory and host system alterable threshold store for storing a value to which those means are coupled are not elements governed by 35 U.S.C. § 112 ¶ 6. The "means . . . for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41); "**early transmit logic 6A**" (see fig. 1; col. 4, ln. 11); "**download DMA logic**		Realtek contends that 35 U.S.C. § 112 ¶ 6 governs this claim element and identifies the corresponding structures, acts, or materials as follows: Fig. 2 – threshold logic 36, threshold store 43 Fig. 3 – RAM 15 Fig. 5 – transmit descriptor and download DMA logic 107 Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304, and D-type flip-flops 305, 206 Fig. 12 – start threshold register 320, download

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
numbers: '872 patent: 10	**58**" (see figs. 4, 4A; col. 23, ln. 22); "**11 bit counter 300**" (see fig. 11; col. 23, ln. 30); and "**download bytesResidentValue**" (see fig. 11; col. 24, ln. 9); see also threshold store 43 (fig. 2); network interface processor 14, RAM 15 (fig. 3); transmit descriptor and download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 350, 351, 352, 353, 354, 355, 356, 357 (fig. 16); elements 370, 371, 372, and 373 (fig. 17).		compare clock 321, and immediate data comparator 322 Fig. 13 – threshold registers 330, 331, and threshold valid register 332 Fig. 14 – threshold value state diagram elements 335-37 Fig. 15 – comparator 340, AND gate 341, comparator 342 Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355, comparator 357 Realtek reserves the right to rely on any statement made by any party under the Patent Local Rules.

II. PATENT L.R. 4-3(c): TIME FOR CLAIM CONSTRUCTION HEARING

The parties believe that one day will be sufficient for the Claim Construction Hearing.

III. PATENT L.R. 4-3(d): WITNESSES AT CLAIM CONSTRUCTION HEARING

Pursuant to Patent L.R. 4-3(d), Standing Order 3.2, and the February 14, 2006 teleconference with the Court, the parties understand that the Court will not receive live testimony and/or expert declarations in connection with the briefing and/or hearing on claim construction. However, the parties reserve their rights to provide expert testimonies and expert declarations relevant to claim constructions in later proceedings with the Court or other courts.

IV. PATENT L.R. 4-3(e): OTHER ISSUES FOR PRE-CLAIM CONSTRUCTION HEARING CONFERENCE

The parties have not identified any other issues which might appropriately be taken up at a prehearing conference prior to the Claim Construction Hearing.

Dated: March 31, 2006

Respectfully Submitted,

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Pursuant to General Order No. 45, Section X(B) regarding signatures, I attest under penalty of perjury that concurrence in the filing of this document has been obtained from Elizabeth H. Rader and David M. Barkan.

Dated: March 31, 2006

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